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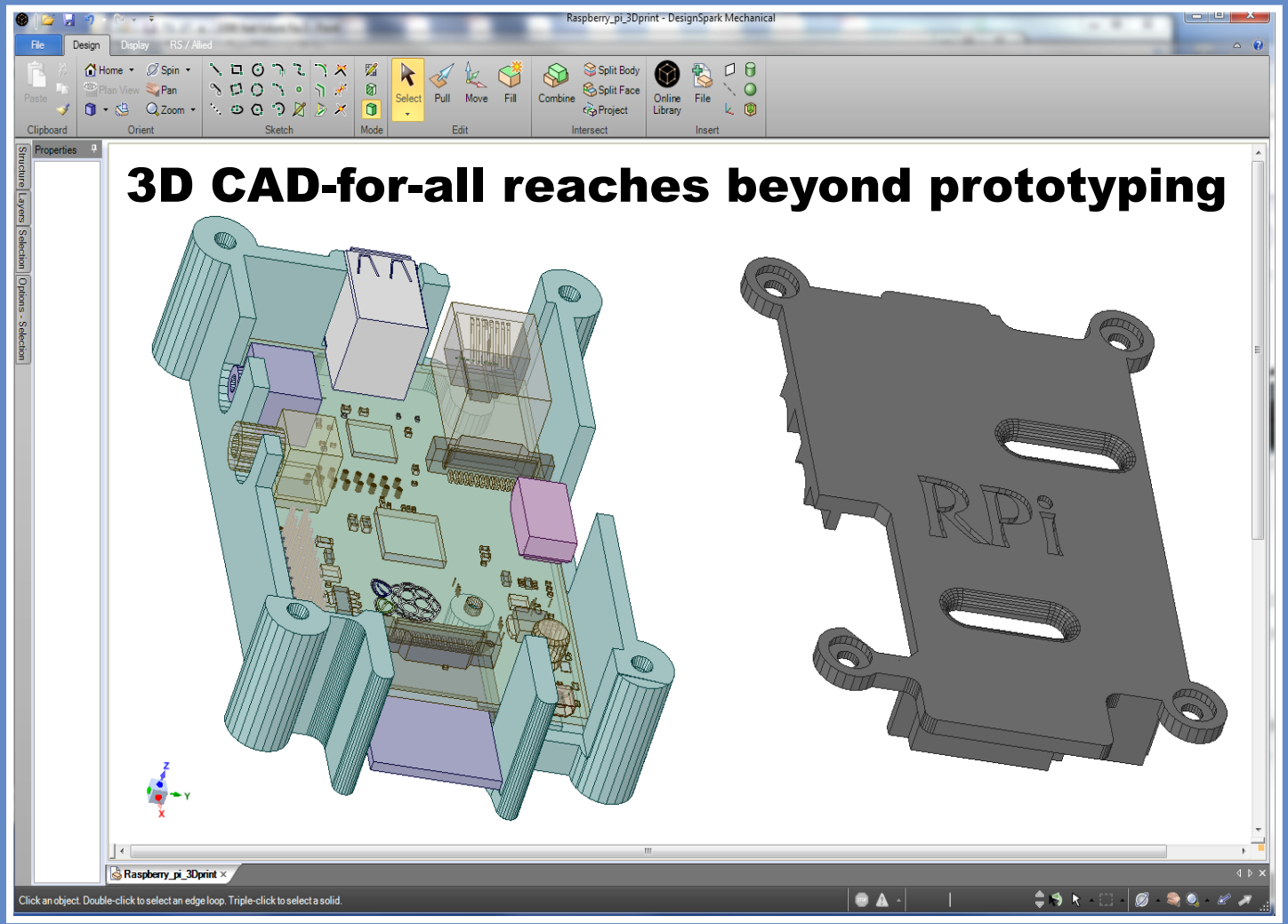

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COVER

3D Design-for-All tool now talks to 'pro' CAD

Distributor RS Components promised that any engineer – not only mechanical CAD specialists – could learn effective 3D mechanical design in a matter of hours. RS' free 3D design package, DesignSpark Mechanical, is aimed at prototyping and targets a 3D printer as its main output. Now, two add-on packages extend the reach of the software into full manufacturing. These are not free but are low cost (see story here); they will enable users to import and export fully-detailed designs into the full manufacturing process, handing files off in common formats. The intention is to, "open up the 3D design process to users who would otherwise not attempt it at all."
The first premium module available is DesignSpark Mechanical Exchange, which adds advanced import/export capabilities and enables the import, modification and export of industry-standard STEP and IGES file formats. The second is DesignSpark Mechanical Drawing, which which allows the changing of designs, as well as the ability to create and modify geometry from within drawing views. It enables the creation of detailed dimensioned drawings allowing designers to move beyond concept development and the 3D printing of prototypes and on to final manufacturing. The image on the cover is RS' stock drawing of a Raspberry Pi and its housing, in the original free package.

FEATUREARTICLES

ONLINE THIS MONTH

Teardown: Moto 360's traditional watch shape forces design compromises
by Brian Dipert, EDN

The Moto 360 is unique among Android Wear-based smart watches for its circular face... which compelled some design compromises.

EDN's columns

SEMICONDUCTOR M&A: TRYING TO KEEP UP

Recent weeks have seen an upswing in mergers-and-acquisitions activity – much more acquisitions than mergers, to be accurate, in this round – in the semiconductor sector. It has never been entirely clear why these events seem to come in bursts, but this time round several significant names have been in play over a short period. Most recently, it was Intel and Altera. The close co-operation between the two over some time has, of course, been well-known, and Altera had previously disclosed that flagship parts in its 'generation 10' series would be built on Intel TriGate technology (since clarified in a subsequent announcement, here). Also, Intel is understood to be exploring the possibilities of a convergence of Altera's programmable technology with some if its own: accordingly, there has been a thread of "will they/won't they" commentary over many weeks. So, now they will, and according to the corporate statement, "The combination is expected to enable new classes of products that meet customer needs in the data center and Internet of Things (IoT) market segments. Intel plans to offer Altera's FPGA products with Intel Xeon processors as highly customised, integrated products." Which doesn't tell us anything we could not have guessed for ourselves, but hints at some intriguing technology avenues that might open up.

This followed shortly after the announcement of the intended purchase of Broadcom by Avago - and that had been anything but public prior to the deal being revealed. Avago has been one of the industry's lower-profile operators – it was originally, readers might recall, the in-house semiconductor operation of Hewlett-Packard before the instrumentation division of HP split to become Agilent; in 2005 it was in turn spun out of Agilent as Avago, but that abbreviated history gives few hints as to the virtually-continuous process of re-shaping its product portfolio – including by acquisition – that it has followed. To date, however, nothing on the scale of the Broadcom acquisition, which all-but-doubles its size. According to analyst IHS, in non-memory ICs, the new Avago will be third only to Intel and Qualcomm, forming a "dominant presence" in communications and storage ICs... [and] commanding 40% of the wired communications IC market.

And, those bids came only weeks after Microchip's purchase of Micrel; and that in turn, shortly after the NXP/Freescale deal. Which is another one that is tricky to call as definitively being an acquisition or a merger. Of the Microchip/Micrel move, here is my US colleague Steve Taranovich; "Sanghi [Steve Sanghi, Microchip CEO] and team have made some really great moves and have managed to strengthen and expand their position in the industry. Now with the Micrel acquisition, they add new capabilities as well as synergistic products that again complement as well as strengthen the Microchip portfolio. I like this acquisition the best in recent years that Sanghi has made. The Supertex acquisition in early 2014 gave Microchip a high voltage capability it did not have well above the 60V existing levels. Sanghi said that they would now be able to connect an IC across a 1,000V line directly as well as operate well in the 110V environment. In 2012 they acquired Standard Microsystems, a mixed signal connectivity company with a rich IP portfolio also having strength in the automotive infotainment sector, whose revenue boosted Microchip overall financial numbers in mid-2014. They got into Wi-Fi and Bluetooth with the 2012 acquisition of Roving Networks."

As ever with M&A activities, the challenge for all of these players is to make their new combined operations work; to yield, in each case, something that is greater than – and not less than – the sum of the constituent parts. History has shown that, not only is that a tough trick to pull off, but it's an entirely different problem when the deal is (in effect) a big fish swallowing a small one, compared to a coming-together of nearly-equals. On the other hand, and looking at how we got the semiconductor industry we have today, it's pretty much business as usual.

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4x digital zoom	Insulation resistance: Up to 260 GΩ	Supports up to 20 models of Keysight handheld meters
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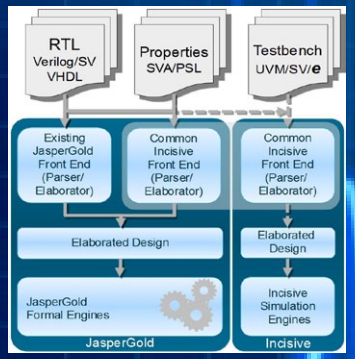
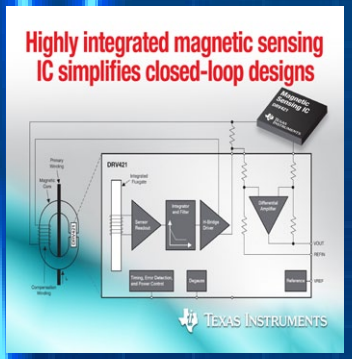
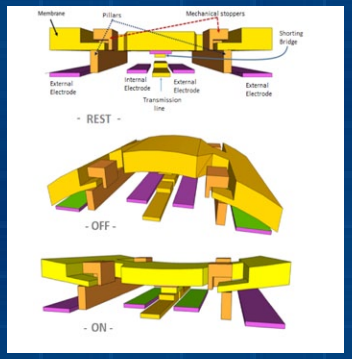

RTL
Verilog/SV
VHDL
Properties
SVA/PSL
Testbench
UVM/SV/e
Existing JasperGold Front End (Parser/ Elaborator)
Common Incisive Front End (Parser/ Elaborator)
Common Incisive Front End (Parser/ Elaborator)
Elaborated Design
Elaborated Design
JasperGold Formal Engines
Incisive Simulation Engines
JasperGold
Incisive


Highly integrated magnetic sensing IC simplifies closed-loop designs
Texas Instruments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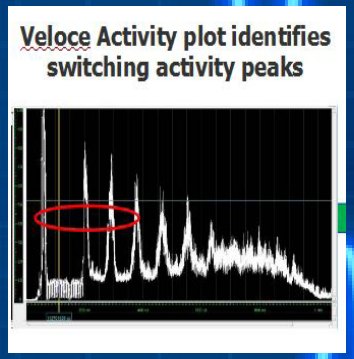
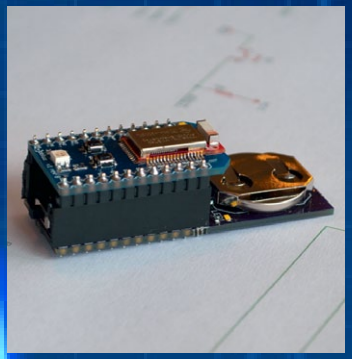
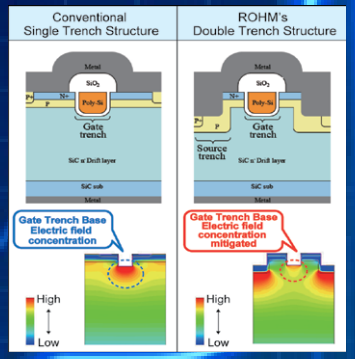
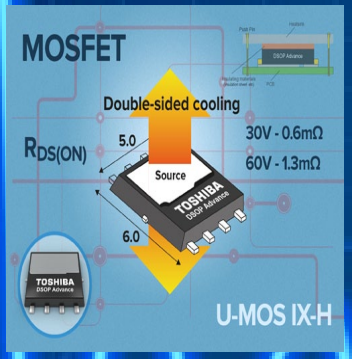
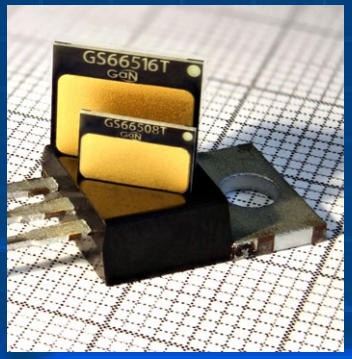
EPC2033/2034
150/200 V eGaN® FETs

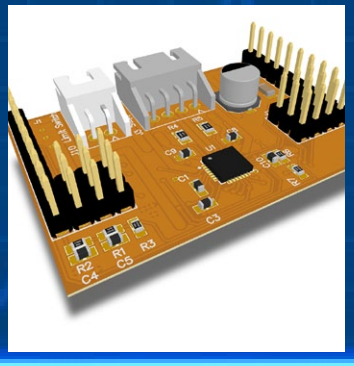

Veloce Activity plot identifies switching activity peaks

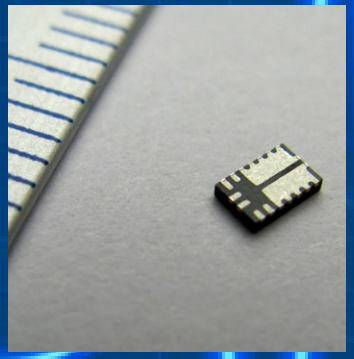


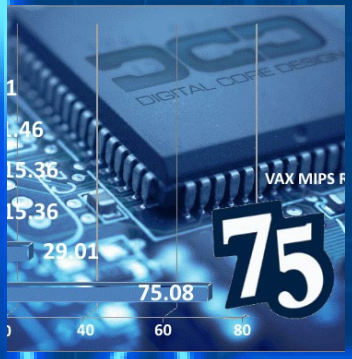

Conventional Single Trench Structure
ROHM's Double Trench Structure
Gate trench
Source trench
Gate Trench Base Electric field concentration
Gate Trench Base Electric field concentration mitigated
High
Low


MOSFET
Double-sided cooling
RDS(ON)
5.0
6.0
Source
30V - 0.6mΩ
60V - 1.3mΩ
TOSHIBA
U-MOS IX-H


GS66516T
GaN
GS66508T
GaN

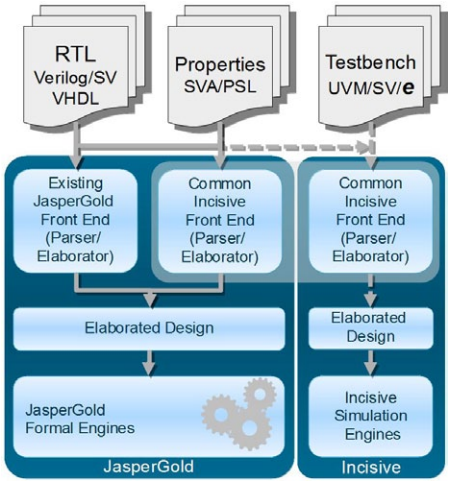





DIGITAL CORE DESIGN
VAX MIPS
75
75.08
29.01
40
60
80

Cadence combines its own, and acquired Jasper, formal tools

Cadence has announced its next-generation formal verification platform. Combining the formal methods previously incorporated in Cadence's Incisive tools with the technology it purchased with Jasper, the designation selected going forward is the JasperGold Formal Verification Platform. Cadence says that while the benefits derived from applying formal methods are highly application-dependent; it is seeing "up to 15X performance gain versus previous solutions", and that JasperGold, now integrated within the System Development Suite, finds bugs typically three months earlier than existing verification methods. The formal analysis engines are now integrated with Cadence's Indago debug platform, automating root-cause analysis and on-the-fly what-if exploration. The performance metric is, essentially, the number of formally-expressed properties completed (or disproved) in a given time.



A Cadence spokesman commented that broadening the use of formal methods is about both performance and usability, and notes in particular the integration of formal methods into the debugging process to use the techniques more generally. The "classic view" of formal methods is that of forming a complete and rigorous proof that (to take the case of logic equivalence checking) one representation of a desired function is identical in every respect to another: that one does exactly the same, no more or less, than the other. Completeness is not essential to get value from the tools, Cadence says. The traditional view of the tools' output is that they might tell you that you have, or do not have, equivalence – and might be of limited help in revealing why not, should the test have failed. Cadence says that in its latest implementation the software can – in effect – stop when it encounters a bug and tell the user, 'this is a bug that in itself would prevent reaching completeness'. There is also the possibility of grading issues found by the formal engines according to whether they are ultimately of importance to the functioning of the system. Expansion of the use of the underlying formal 'engines' extends beyond assisted debug into formally-assisted simulation; a range of engines can be applied to a problem, or individual mathematical engines can 'hand-off' problems to each other. A further dimension is formal-assisted emulation, where assertion-based approaches augment [hardware-] accelerated techniques.

Complete article, here

Automotive SoCs targeted by qualified IP from Synopsys

Synopsys' DesignWare IP portfolio includes functions to meet key automotive functional safety requirements and is being further enhanced with availability of ASIL B ready IP, and investment in AEC-Q100 testing and TS 16949 quality management. Synopsys' latest IP announcement is aimed at designers of automotive SoCs; there is a portfolio of IP for automotive applications I the DesignWare series that includes Ethernet Audio Video Bridging (AVB), LPDDR4, MIPI CSI-2 and DSI, HDMI, PCI Express, USB, Mobile Storage, Logic Libraries, Embedded Memories, Non Volatile Memories (NVM), Data Converters, Synopsys ARC EM processors with Safety Enhancement Package (SEP), EV vision processors and the Sensor and Control IP Subsystem. The DesignWare IP portfolio meets key automotive functional safety requirements today and is

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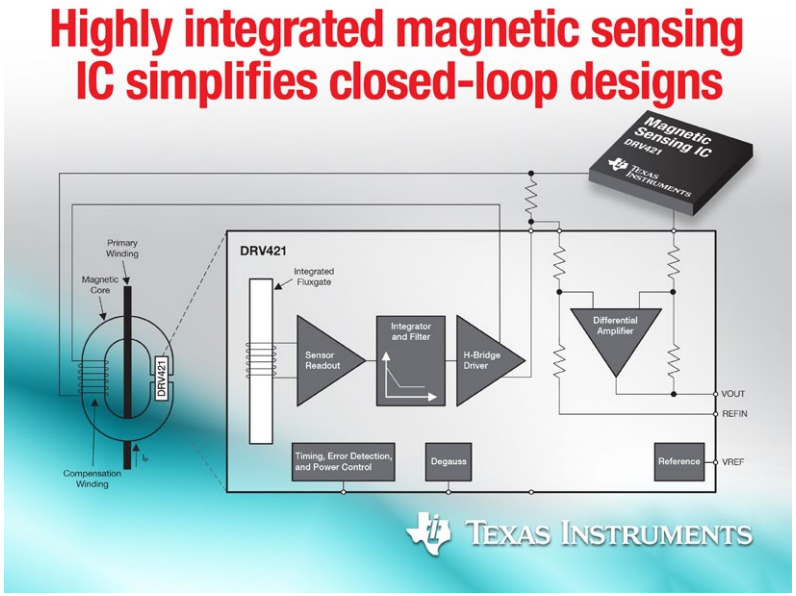
being further enhanced to address AEC-Q100 and TS 16949 requirements. Designers can, says Synopsys, accelerate their functional safety assessments and meet the high quality levels required in automotive applications such as advanced driver assistance systems (ADAS) and infotainment. DesignWare Ethernet AVB, LPDDR4 and Embedded Memory IP are now certified to be ASIL B Ready for ISO 26262 functional safety, as required by ADAS applications. The ASIL B Ready DesignWare IP is delivered with safety packages that include failure modes effects and diagnostic analysis (FMEDA) reports as well as safety plans and manuals, giving designers the documentation needed to complete their own certification processes. In addition to the ASIL B Ready IP currently available, Synopsys offers ARC EM processors with SEP for safety critical embedded applications and the ASIL D Ready ARC MetaWare Compiler.

Complete article, here

Integrated fluxgate sensor provides closed-loop current sensing

With signal conditioning and compensation coil driver in a single package, this device from TI claims high accuracy, dynamic range and linearity, and simplified system design, from a high level of integration. Texas Instruments says this is the first magnetic sensing integrated circuit with a fully integrated fluxgate sensor and compensation coil driver, along with all the required signal conditioning circuitry. Integration enables the DRV421 to provide best-available sensor accuracy and linearity, high dynamic range, and simplified system design compared to traditional closed-loop sensors. TI says that system designers will be able to more easily develop magnetic closed-loop current sensors for applications such as motor control, renewable energy, battery chargers and power monitoring.



The device allows precise control over motors and automation equipment with an overall sensor accuracy of less than 0.1%. It reduces coupling between the compensation coil and the fluxgate sensor, as well as emissions from fluxgate excitation, to provide high linearity. High dynamic range comes from the built-in closed-loop magnetic core degaussing procedure and offset calibration increase dynamic range up to six decades while supporting higher system-level accuracy, compared to traditional solutions. As the first fluxgate sensor supporting 3.3-V operation, the DRV421 simplifies the interface to integrated ADCs on low-power microcontrollers.

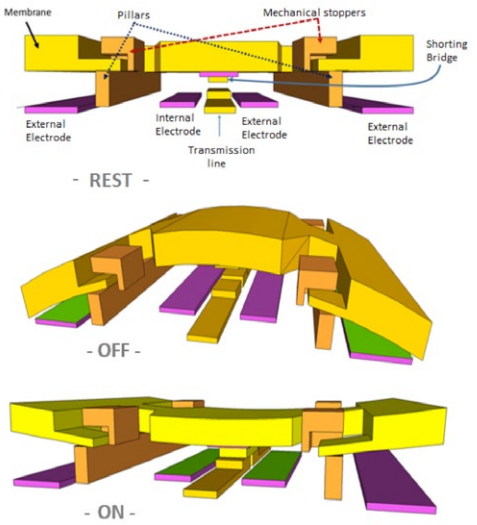
The DRV421 evaluation module (DRV421EVM) enables designers to evaluate the IC, for $49. Sumida Corporation has introduced the SC2912, a magnetic module that system designers can place on top of the DRV421 as a printed circuit board (PCB) component. This allows engineers to design universal platform solutions targeting a wide range of current levels while choosing the appropriate magnetic module for their specific use case.

Complete article, here

RF-MEMS ohmic switch exceeds one-billion-operation lifetime

DelfMEMS has announces that its SP12T, MEMS RF switch has exceeded 10 billion operations while on test, and is still fully functional. The company designed its FreeFlex RF-MEMS technology to outperform current RF switch designs and to deliver the operational performances needed for next generation LTE-A handsets. DelfMEMS says that two innovations help it achieve this breakthrough. First, although gold is currently used as the contact material, this will be replaced in the production switches by a metal compound that has been proven to be reliable for cold switching in excess of 50 billion cycles. Second, its FreeFlex MEMS switch design ensures that the contact point is always changing slightly, which lengthens the life of the switch.

Cybele Rolland, DelfMEMS CEO, comments, "Achieving the billion switch milestone is a major achievement for our FreeFlex design. Importantly, this is the first time an industrialised RF-MEMS contact switch has been show to achieve this level of performance,



but this is only the beginning. Our second-generation production switches, which we will be shipping towards the end of 2016, are expected to achieve up to 50 billion operations. This ensures that they will reliably deliver the performances required for the next generation of handsets, LTE-A and beyond, with ultra-low insertion loss, outstanding isolation and superior linearity."

The DelfMEMS RF-MEMS switch structure uses an integrated, micro-mechanical building block that is based on an IP portfolio that includes seven key patents and innovations. It does not use a cantilever beam or bridge [that employ] a highly conductive electrode electrostatically actuated in order to create an ohmic contact resulting in a mechanical switching. These older structures (the company adds) proved to have several issues: stress on the anchors, possible stiction, low commutation speed and possible creep of the beam.

DelfMEMS' design approach has resulted in the development of an anchorless structure for mechanical RF switching which overcomes these historical design problems instead of trying to simply reduce them.

Complete article, here

EPC adds 7 mΩ/200V, and 5 mΩ/150V GaN power transistors

Efficient Power Conversion (EPC) says it has "widened the performance gap" by introducing its latest gallium nitride power transistors; lower on-resistance, lower capacitance, higher current, and superior thermal performance enable high power density converters, the company asserts.

These eGaN FETs – enhancement-mode, or normally-off – have a maximum operating temperature of 150°C and pulsed currents capabilities of 260A (150V EPC2033) and 140A (EPC2034). Applications include DC-DC converters, synchronous rectification in DC/DC and AC/DC converters, motor drives, LED lighting, and industrial automation.

In a recent conversation with EDN Europe, EPC CEO Alex Lidow commented on the progress of GaN, "I said five years ago that we would deliver devices at lower cost than equivalent silicon [tran-

sistors] – now we have done that, with parts in the 100V and 60V ranges. For equivalent performance, [and even at low volume] in one-off or in 1000s, we have parts priced less than the silicon equivalent." Lidow comments that the lower losses of GaN allow like-for-like electrical parameters to be achieved with smaller dice, and [once routine volume production is established] at lower costs. He emphasises that the parts he describes are not "loss leaders", "We're a start-up, still a small company – we can't do that."

In terms of making GaN a larger part of the power control market, Lidow believes that device technology is now in place; what is not there? "The supporting silicon," he says, referring to functions such as driver ICs, "isn't fast enough to make use of the speed of GaN. The pace is being set by the control ICs, in areas such as wireless power and LiDAR."

In December's EDN Europe we carried an item on testing to evaluate the real speed of samples of EPC devices: Alex Lidow says that others making the same assessments have had to develop specialised test fixtures and methods to resolve power switching waveforms at 200 psec or better, "You can't do that with the device in a package, with gate connection inductances over 100 pH."

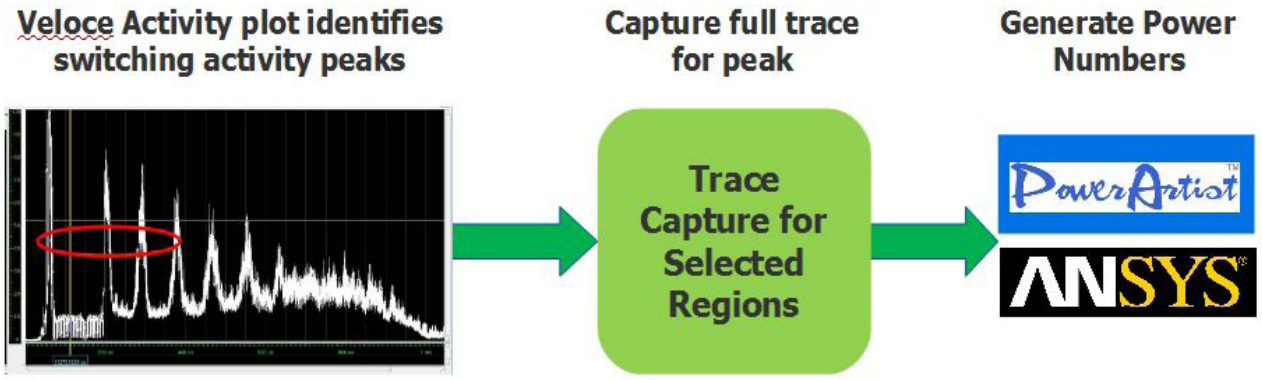
The products in the present announcement join EPC's family of "Relaxed Pitch" devices featuring a 1 mm ball pitch. The wider pitch allows for placement of additional and larger vias under the device to enable high current carrying capability despite the small 2.6 x 4.6 mm footprint. Parameters of the new parts are, respectively for the EPC2033 and 2034; V_{DS} of 150/200V; $R_{DS(on)}$ of 5.0/7.0 mΩ; Q_G of 10/8.5 nC; and priced (1000) at $4.25/$4.37

Alex Lidow offers a further prediction for his market sector; "In 5 years from now, the most significant driving force [in power conversion] will be wireless power... power cords are the last cord we have, the data connections have gone wireless, next is the turn of the power [connection] – computers with no cords at all."

Complete article, here

Mentor refines power prediction in complex SoC designs

Users of Mentor Graphics' Veloce emulation systems now have a more detailed and more accurate method of predicting power consumption of a large-scale IC. The Veloce Power Application uses actual OS and application behaviour, via the hardware emulation vehicle, to identify and zoom in on blocks in the design that are generating power peaks. The Veloce Power Application, Mentor says, delivers a complete solution that enables a new comprehensive methodology for power, embodying accurate and early switching activity at the application level. Users can carry out early budgeting and tradeoff exploration at RTL; and analysis and sign off at the gate level. Real-time transfer of power switching activity, via a Dynamic Read Waveform API, to power analysis tools replaces current file-based activity transfer methodology – this



feature employs close integration with third-party power analysis tools

Mentor Graphics' starting point is that a new usage model for handheld and smart devices is driving a methodology shift in the way power is analysed; the company cites Qualcomm as having made a significant input into the desired feature list for this software. One primary driver in this shift is the fact that complex SoC designs are now verified using live applications that require booting the OS and running software applications on an emulator. It is more effective to use the power switching activity plot, generated during emulation, to pass real-time switching activity information to power analysis tools where potential power issues can be evaluated.

When this is done today, Mentor says, the default approach is to boot designs that are heavily software- or application-driven on the emulator, then generate output files of activity which can then be read by a downstream power analysis tool. Issues around this approach are that for meaningful application (or even OS) runs, files can be unmanageably large, and the analysis tools can take unacceptable time to read them – if reading them is even practical. In this release, Mentor provides a means of identifying power peaks in the SoC's (or its constituent blocks') demand, and writing out only the intervals that see the critical power peaks. Further, via an API, the data is copied directly to the downstream analysis tool, rather than via a file. The file-based power analysis flow is replaced by a Dynamic Read Waveform API integration to power analysis tools. This enables accurate power calculation at the system level, better power exploration at RTL for power budgeting and tradeoffs as well as more accurate power analysis and sign-off at the gate level.

The result, Mentor says, is a significant boost in runtime and performance. The typical approach of running the emulator, creating the file, reading the file into the power analysis tool and running the power analysis tool is now, with this new approach, reduced to the emulator and power analysis runtimes. Mentor adds that early users have seen up to a 4.5X runtime performance improvement.

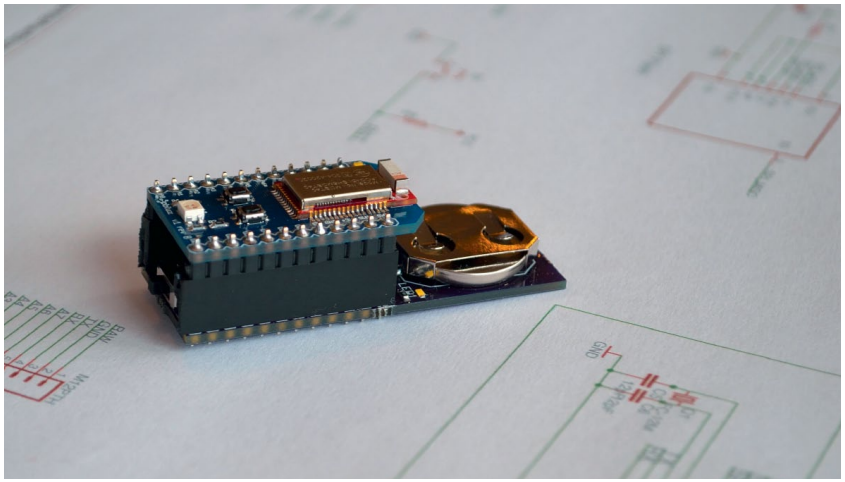
Complete article, here

IPv6 Bluetooth Smart IoT dev kit comes cloud connected

The result of a Kickstarter campaign that far exceeded its original funding, the Bluz Bluetooth Smart development kit comprises an Arduino-style stackable prototype board, hosting a Nordic Semiconductor nRF51822-based module, that allows users to build almost any cloud-connected Bluetooth Smart IoT application from scratch

The IPv6 compatible Bluetooth Smart (formerly known as Bluetooth low energy) Internet of Things (IoT) development kit, Bluz, has been developed by U.S. startup Easier To Use. It employs a Nordic nRF51822 System-on-Chip (SoC) based module and offers cloud-connectivity out-of-the-box. Bluz is marketed as a basic Bluetooth Smart, Arduino-style, Spark Core/Photon pin-compatible platform designed to enable anyone to build low cost, ultra low power IoT devices that can operate from

a coin-cell battery for months or years using an expandable set of stackable printed circuit board shields to add further functionality. Developer Easier To Use says cloud-connectivity is provided by a Wi-Fi dongle or - for wearables - a user's Bluetooth Smart Ready smartphone (via cellular network tethering) powered by low cost cloud-connectivity specialist Spark and compatible with app-based product control services such as IFTTT and Tinker for triggering events and processes.

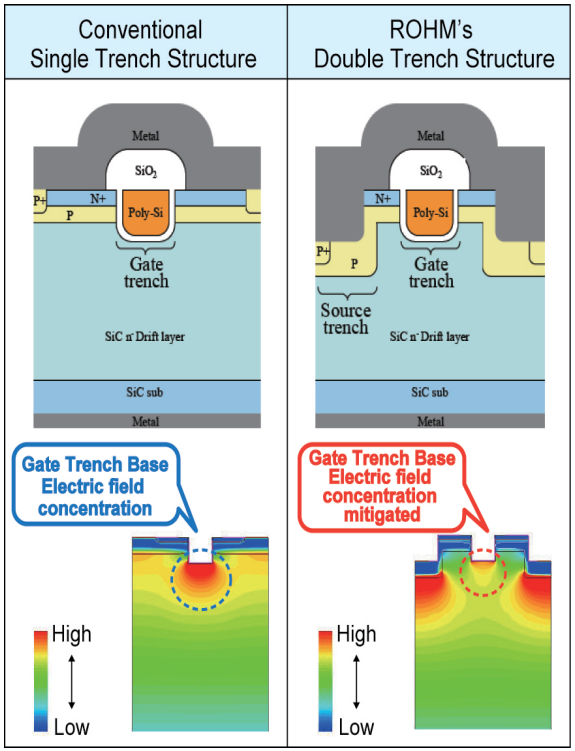


By combining with Spark, Easier To Use says that Bluz is able to be controlled completely from the cloud. This includes the ability for the hardware to be accessed through a simple REST API when it is online and programmed over the air from anywhere. Easier To Use says Bluz will also integrate seamlessly into the Spark ecosystem, so it will be programmable through the Spark Web IDE and will work with all other features of the Spark ecosystem (including Webhooks, Dashboard, and Tinker). Bluz itself is a standalone board that is said to break out all the major functions of the Nordic nRF51822 (such as SPI, I²C, and UART) as well as 18 GPIO pins. Easier To Use says that Bluz can also be paired with a number of stackable shields, such as an accelerometer, battery, or prototype shield to allow quick and easy creation of custom prototypes.

Complete article, here

First trench-type SiC MOSFET cuts on-resistance

Rohm Semiconductor has recently announced the development and mass production of a silicon carbide (SiC) MOSFET that it claims as the first such transistor to use a trench structure. Compared to existing planar-type SiC MOSFETs, ON resistance is reduced by 50% in the same chip size, making it possible to significantly decrease power loss.



The very high stability of silicon carbide makes it difficult to form deep structures within its crystal lattice; Rohm says it has overcome these limitations to produce a device that combines very low loss with high-speed switching performance. Rohm adds that the company is developing full SiC modules that integrate both SiC MOSFETs and SBDs.

The company notes that with the trench structure, a MOSFET gate is formed on the sidewall of a groove created on the chip surface. Unlike planar-type MOSFETs, JFET resistance does not exist, making greater miniaturisation possible. This is expected to result in ON resistance close to the theoretical limits of performance of the SiC material. Although adopting a trench con-

struction in SiC MOSFETs has been attracting increased attention due to its effectiveness in reducing ON resistance, there is a need to establish a structure for mitigating the electric field generated in the trench gate portion in order to guarantee long-term reliability. Rohm says it has overcome this limitation and can successfully mass-produce the first trench-type SiC MOSFETs with improved switching performance (approx. 35% lower input capacitance) and ON resistance reduced by 50% over planar-type SiC MOSFETs. The lineup is being expanded to include 3 models for each rated voltage: 650V and 1200V, with rated currents of 118A (650V) and 95A (1200V). ROHM has also developed a full SiC power module that incorporates these latest trench-type SiC MOSFETs in a 2-in-1 circuit with integrated SiC SBDs.

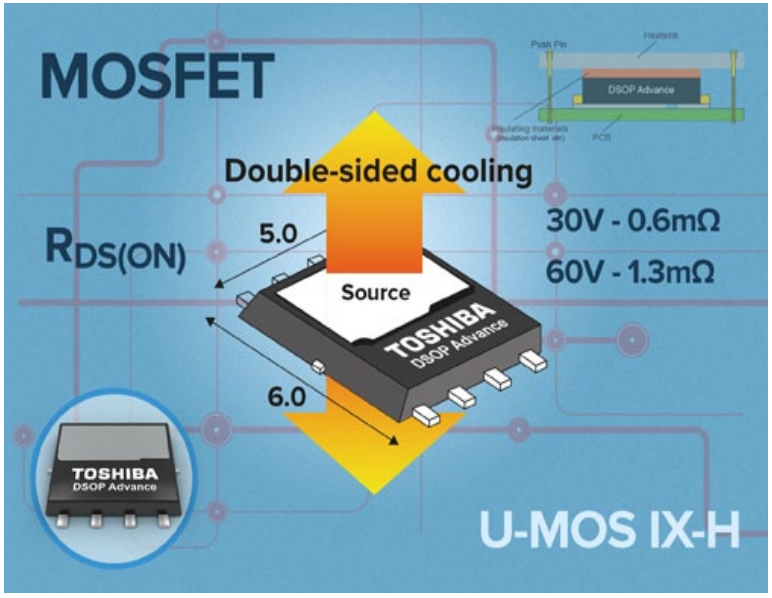
Complete article, here

Double-sided cooling package for Toshiba's 30/60V power MOSFETs

Toshiba has expanded its ultra-high-efficiency MOSFET family by adding 30V and 60V devices with dual-sided cooling options; these FETs use the company's U-MOS IX-H trench process deliver high efficiency at all loads and are available in miniature DSOP advance package.

The 30V and 60V devices join the company's existing 40V offering. All of the devices will be available in ultra-compact, thermally efficient DSOP Advance package options that significantly improve heat dissipation through dual-sided cooling.

The package directly attaches copper tabs to the top (source) and bottom (drain) of the die, and makes the outer surface of each piece of copper available on the top and bottom faces of the package, where you can directly mount a heatsink with low thermal resistance. Care will be needed in mechanical/insulation design, as any projection of the heatsink beyond the package edge will mean that drain and source potentials may be physically separated by only the package thickness.



Comprising one 30V device and one 60V device, the new N-channel MOSFETs are based on Toshiba's next-generation U-MOS IX-H trench semiconductor process. This process has been designed to deliver optimum efficiency across a wide range of load conditions by reducing on-resistance ($R_{DS(ON)}$) and improving switching efficiency by reducing output charge (Q_{OSS}).

Toshiba aims the MOSFETs at power management circuits including high-side and low-side switching in DC-DC conversion and secondary side synchronous rectification in AC-DC designs. The technologies are also suitable for motor control and for protection circuit modules in electronic equipment based on Lithium ion (Li-ion) batteries.

At a voltage (V_{GS}) of 10V, the maximum $R_{DS(ON)}$ rating for the 30V MOSFET is 0.6 mΩ, while typical C_{OSS} is 2160 pF. The 60V item offers $R_{DS(ON)}$ and typical C_{OSS} ratings of 1.3 mΩ and 960 pF.

Complete article, here

Formal verification company provides technology access on "app" model

Formal verification has long held promise as a verification tool for the SoC design chain – but the arcane nature of the applied mathematics involved has limited its use to a subset of specific areas. German specialist OneSpin Solutions has now found a way that third parties can build tools on the base of its formal verification "engines", applying the full power of the technology while retaining full secure over its underlying formal intellectual property.

The new vehicle is OneSpin 360 LaunchPad, which the company terms the "first Adaptive Formal Platform"; partner companies will be enabled to use the power of formal verification in a range of verification solutions that they can position, market and price according to their own models – all without (necessarily) understanding the subtleties of the formal technology itself.

LaunchPad is a complete formal environment that can be applied by app developers without in-house formal technology or expertise. Domain experts can create formal-based solutions targeting verification tasks that lie within their specific field on a proven underlying verification foundation. LaunchPad may be delivered as part of the app by the developer. Or, the app can be included in the OneSpin App Library to operate with the company's formal product line.

The platform that OneSpin has developed employs encryption and key-based security. When the solvers are distributed as part of an app, they will only recognise data generated by and within the app; and the technology of the verification engines themselves is not visible to the end user.

"LaunchPad is a missing link in the widespread adoption of formal verification, and will extend the reach of powerful formal techniques into new areas," says Dr. Raik Brinkmann, OneSpin Solutions' president and chief executive officer (CEO). "The pre-existing platform makes it easier and quicker for domain experts to develop a robust verification solution suitable to their market segment, without the need for acquiring in-house formal knowledge or technology."

OneSpin adds that the apps that its partner companies develop can provide in-depth, specific verification solutions in an automated fashion, often eliminating the need for end users to write assertions while improving ease-of-use. Previous practice – even in cases where an "app-like" tool has been created – has been to build them into the formal tool itself: so they could only be delivered by the formal verification tool vendor who then had to have not only the comprehension of formal techniques, but had also to acquire domain-specific knowledge. LaunchPad eliminates this requirement by encapsulating a complete formal platform in a manner that allows its easy integration into a variety of specialised systems by engineers without a formal technology background – but with the required familiarity with their own areas.

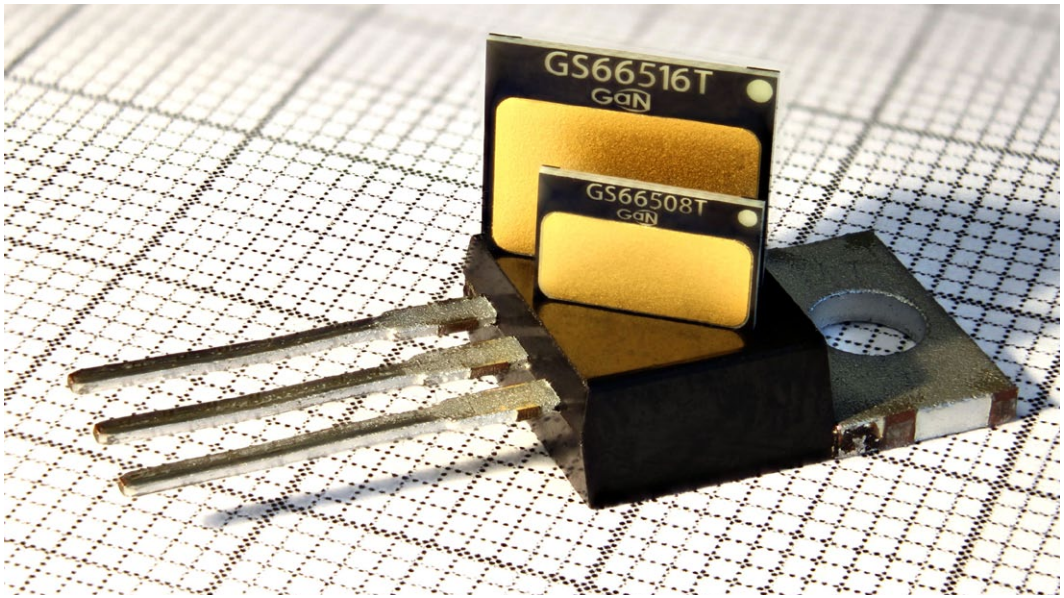
This broadens the scope of formal verification to a range of disciplines previously closed to the technology, OneSpin says. Through the use of SystemVerilog-based standards to create an easy integration methodology, LaunchPad can be applied quickly and in an open manner. Because LaunchPad only works with the integrating app, the business model to the end-user can be set to match the app itself.

Complete article, here

GaN Systems' 60A power transistor sets high point in current handling

The gallium nitride device maker claims to now have the highest current GaN power transistor on market at 60A. The GS66516T high power transistors based on its three core proprietary technologies.

The GS65516T 650V E-mode



650V E-Mode power switch with top side cooling, low inductance GaNPX packaging and ultra low figure-of-merit Island Technology suits high frequency, high efficiency power conversion. GaN Systems has added the part to its range of E-mode GaN-on-Silicon power switch features GaN Systems' topside cooling configuration announced in March this year, which allows the device to be cooled using familiar and conventional heat sink or fan cooling techniques. It is based on the company's Island Technology die design, packaged in low inductance and thermally efficient GaNPX packaging and measures 9.0 x 7.6 x 0.45 mm. Features of the GS65516T 650V E-HEMT include reverse current capability, integral source sense and zero reverse recovery loss. Dual gate pads help design engineers achieve optimal board layout. The GS65516T suits high frequency, high efficiency power conversion applications such as on-board battery chargers, 400V DC-DC conversion, inverters, uninterruptible power supplies (UPS) and VFD motor drives, AC-DC power supplies (PFC and primary) and VHF small form factor power adapters.

"GaN is real and happening right now," according to Girvan Patterson, President, GaN Systems. "... hundreds of leading companies across the globe have embraced our technology to make sure they are among the first to market with new products that bring the benefits of GaN to products ranging from solar inverters to ultra-slim TVs."

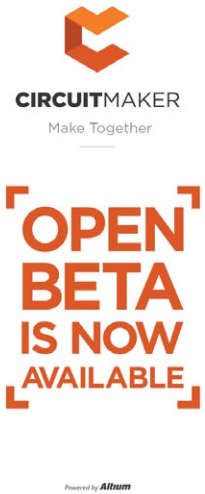
Complete article, here

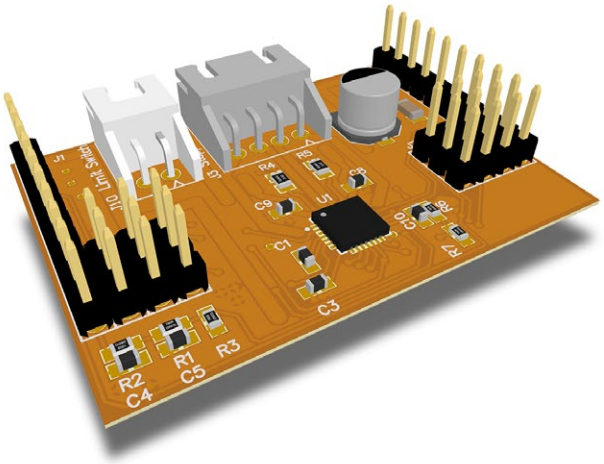
Altium sets up open Beta programme for community-driven, free PCB design tool

The latest stage in the development of Altium's CircuitMaker is to make it available for Use worldwide as part of an open beta testing programme. CircuitMaker will be available worldwide to all interested electronics designers, and aims to address the specific needs of the electronics maker and hobbyist community with a free software offering. All those interested in participating in the open beta can register now at the CircuitMaker website.

"We're excited to see how the CircuitMaker community will grow and evolve during this open beta program," said Ben Jordan, Product Manager at Altium. "The electronics maker community has always been characterised by a very organic and collaborative growth process, and now electronics designers at all scales have Cir-

cuitMaker with which to voice their creativity."
Altium adds that the growth of the electronics maker community has created a niche market and, the company believes the need for a specialised PCB design tool.





Altium has committed itself to addressing the need of this growing community with a PCB design tool focused on open hardware and shared design resources.
The open beta testing program allows anyone to download and begin using CircuitMaker today and become part of a growing electronics design community where designs can be shared and collaborated on. This open beta process will also provide feedback and input to refine CircuitMaker, for electronic designers in the maker community.
CircuitMaker will be available at no cost to anyone interested in using the software, with no limits to design capability. Altium says that the PCB design tool offers a, "polished and streamlined" design tool for the maker community with features such as: comprehensive PCB design technology; advanced community collaboration; and a streamlined interface.

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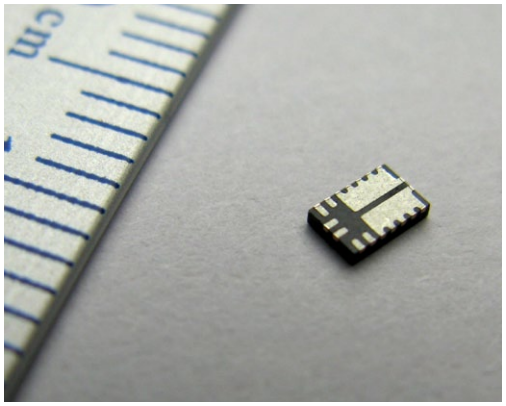
Self-contained 3.8 mΩ/10-A high-performance power switch

Silego Technology's SLG-6M6201V is a self-contained 3.8 mΩ power switch optimised



for 3V to 3.6V power distribution and designed to handle continuous load currents up to 10A.
Based on its CurrentPAK technology, the SLG6M6201V is Silego's first fixed-configuration version of its NVM-programmable CurrentPAK Configurable Mixed-signal IC, or CMIC.
The preceding SLG6M6001V offered full programmability of multiple IC parameters using built-in NVM (Non-Volatile Memory). SLG-6M6201V simplifies high-power, 3V power distribution in server and RAID systems by, firstly, setting the output voltage slew rate at 1.6 V/msec to control power-rail in-rush current profile, as well as minimising downstream RFI, while also setting the internal VOUT discharge feature to 300Ω to speed up the discharging of distributed, output capacitive loads, and finally by providing VOUT power-good output signalling to indicate to downstream DC/DC converters and system controllers that the power rail has reached 90% of final value.
The SLG6M6201V offers the system designer the ability of setting the power switch's dual-level active current limit at 1.25A or 12.5A through an external pin for improved over-current detection in low- or high-load current applications. In an 18-pin 2.0 x 3.0 mm STQFN package, the SLG-6M6201V is fully specified from -10°C to 70°C.

Complete article, here

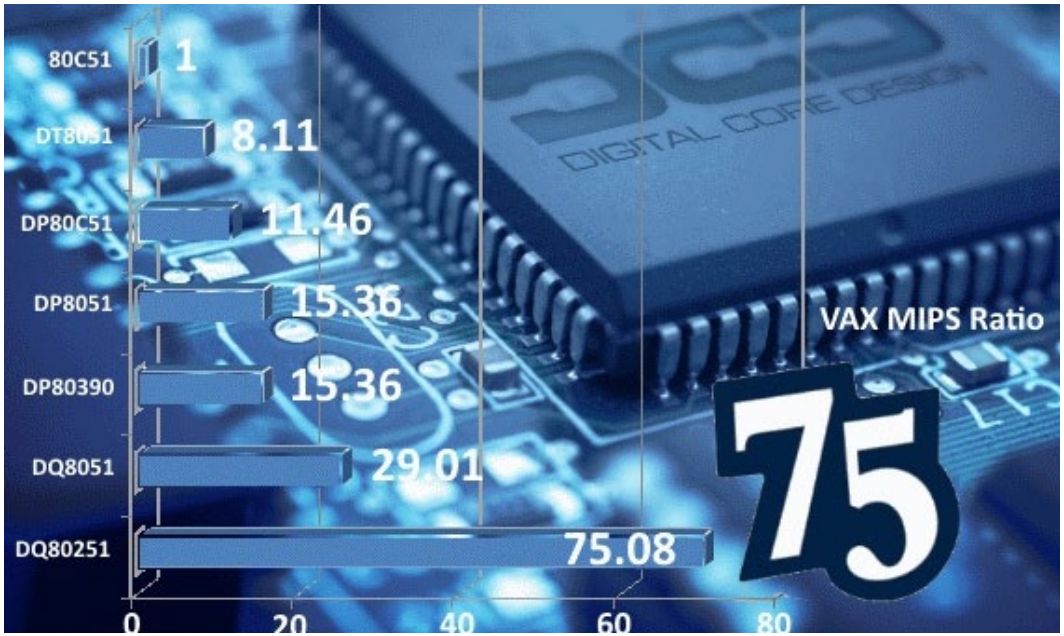
Analog Devices' AD7177-2 32-bit ΣΔ ADC, in distribution

Mouser Electronics has the AD7177-2 32-bit sigma delta analog to digital converter (ADC) from Analog Devices. AD7177-2 is a low noise 32-bit sigma delta (Σ-Δ) ADC with a true rail-to-rail input buffer and flexible scan rates. This 32-bit ADC can be configured as two fully differential, or four single-ended, analogue inputs with a channel scan rate of 10 ksamples/sec. The AD7177-2 is designed to operate as a fast settling, very high resolution, Σ-Δ ADC with high levels of configurability.
Intended for applications that require the measurement of very high precision analogue data, the AD7177-2 can also be configured for 24-bit resolution, which provides faster conversion speeds. The AD7177-2 has four independent channels with four independent setups. Developers can select any of the analogue input pairs on any channel, as well as any of the four setups for any channel, providing full flexibility in the channel configuration. This also allows per channel configuration when using differential inputs, as well as single-ended inputs. A precision 2.5V low drift (2 ppm/°C) band gap internal reference with output reference buffer reduces external component count. Integrated true rail-to-rail buffers on the analogue inputs and external reference inputs allow the ADC to drive high impedance inputs. An SPI interface allows configuration of many of the ADC options including 32- or 24-bit resolution, power down modes, gain, offset calibration values, conversion delay, and enabling the internal temperature sensor. This ADC is specified over the extended industrial temperature range of -40°C to +105°C.

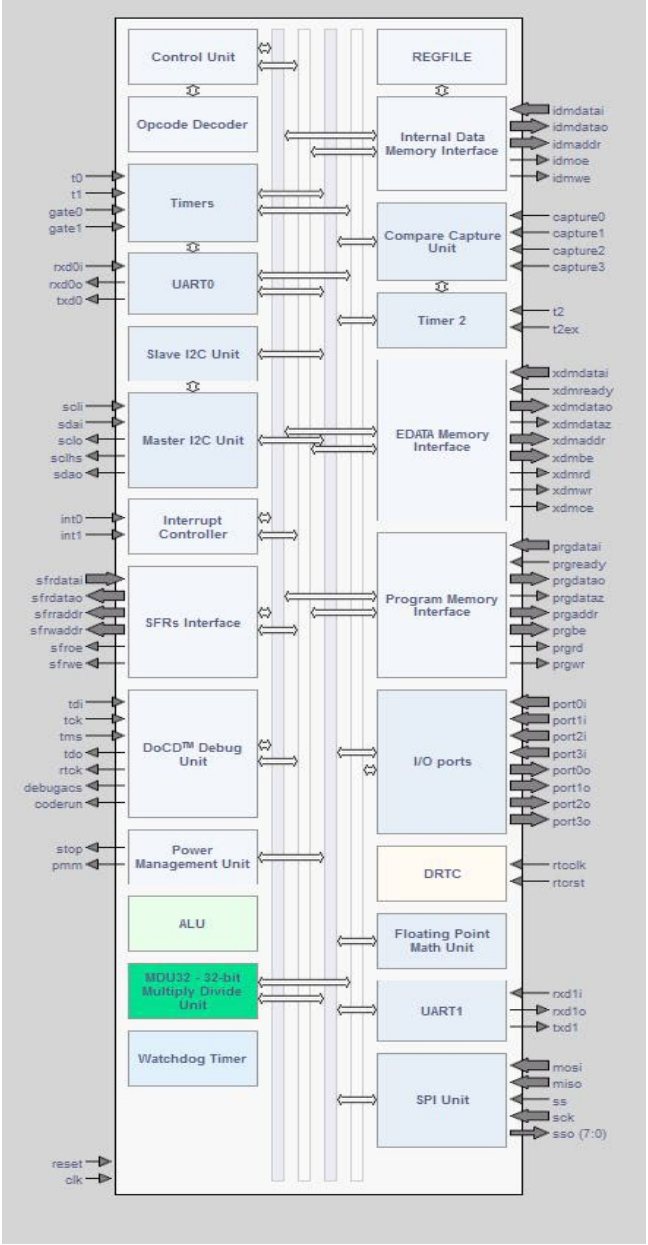
Complete article, here

Fastest 8051 CPU in IP form runs 75x original

DQ80251 from Polish IP vendor Digital Core Design now runs more than 75 times faster than the original 8051 chip, claimed as the highest performance MCS51 instruction set compatible IP Core currently available. This fully configurable 80251 Microcontroller Core executes the MCS-51 and MCS-251 instruction sets and is delivered with a variety of integrated peripherals such as USB, Ethernet, I²C, SPI, UART, CAN, LIN, HDLC and Smart Card.



Digital Core Design launched its first version of the DQ80251 in 2011, offering performance 66 times faster than the original 8051 chip; this version uprates that to execute MCS-51 and MCS-251 instruction sets 75.08 times faster than the original chip. The



DQ80251 boasts a Dhrystone 2.1 performance rating of 0.70579 DMIPS/MHz, which therefore enables a 75.08 times speed-up over the original 80C51 chip operating at the same frequency. The DQ8051's dynamic power consumption is also very low. It rivals not only all other 8051-compatible cores but also low-power 32-bit processors.

The DQ80251 is a royalty-free, cost-effective 8051 IP Core with ultimate code density and instruction intelligence. DCD enhanced the core's functionality by implementing a variety of integrated peripherals, and to enable more complex SoCs design, the DQ80251 is equipped with built-in on-chip debugger (DoCD). It is a real-time hardware debugger, which provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the DoCD provides non-intrusive debugging of a running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals.

DCD says that 8051 CPUs can take a place in high-demand products, thanks to plenty of horsepower and many advantages such as low costs, energy and area, also, the DQ80251 is easy to integrate and program.

Complete article, here

Quantum computing is "closer than you think" - now it has an OS

Cambridge Quantum Computing ("CQCL"; Cambridge, UK) has announced that it has developed an operating system for Quantum Computers. t|ket> is a unique quantum computing operating system; thus far, it has only run on a simulation of a quantum computer, which itself runs on a proprietary custom designed high speed super computer, also built by CQCL, in order to simulate a quantum processor.

A quantum computer takes advantage of quantum interference, and potentially gains an immense advantage in computational speed over conventional computers by being capable of carrying out massive parallel computations simultaneously. The company stated, "CQCL is at the forefront of developing an operating system that will allow users to harness the joint power of classical super computers alongside quantum computers. The development of t|ket> is a major milestone. "Quantum computing will be a reality much earlier than originally anticipated. It will have profound and far-reaching effects on a vast number of aspects of our daily lives."

In addition to t|ket> CQCL is focussed on developing quantum algorithms and software applications in cryptography, financial services, simulation optimisation and genome analysis.

Complete article, here

5,000 METER ALTITUDE PERFORMANCE; CAN YOUR SUPPLY REALLY MEET THIS REQUIREMENT?

By Shane Callanan, Excelsys Technologies

More and more data sheets are now specifying conformity of a power supply for operation at 5,000 metres. However, it is not sufficient to simply derate for lower density of air at higher altitudes. This article will look at the in-depth requirements for higher altitude compliance of a power supply, and will advise the reader on the questions that need to be put to your power supply vendor to ensure compliance for higher altitude operation.

As companies increasingly make a strategic decision to target emerging markets around the globe, an emerging – and real – requirement is for operation up to 5,000 metres above sea level. In many cases a mistake is made by over simplifying the requirements for product compliance for higher altitude operation. It is not enough to only consider derating the maximum power delivered: the user must consider in detail, the design criteria of the power supply they intend to use.

Why the need to derate?

As you go higher from sea level, the density of air decreases. For supplies that use fan cooling, the ability of the fan to cool is significantly reduced. Put simply, the equivalent volume of air moved through the supply, and over its heat-generating components, contains fewer air molecules that can absorb the thermal energy. This is why you must consider derating of power supplies as you increase the altitude. This is both a well-understood and documented phenomenon; as a general rule of thumb you should derate by 10% for each 1,000m you go above sea level. However, what may not as well understand by end users, but is just as important, is the creepage and clearance designed into the power supply.

What is creepage & clearance?

During production testing, power supplies are subject to hi-pot testing. During this test process, a high voltage is applied between specific points on the power supply. Typically, these tests are applied from input to output, input to earth, and output to earth. What we trying to achieve here is to establish that;

1. There is no dielectric breakdown on the power supply
2. We adhere to creepage and clearance requirements of the power supply

Clearance distance can be defined as the minimum distance between two conductive parts, when measured though air. It is this clearance distance between two points that prevents breakdown due to the ionisation of air. EN60950 provides guidance on minimum distances, but as an example you should expect to see 8 mm between primary and secondary circuits at sea level. As you increase in altitude, there is a direct correlation between increasing altitude and the minimum potential needed for dielectric breakdown to occur, which is why the relevant distances need to be increased. Again, EN60950 provides clear direction on what this scaling factor should be.

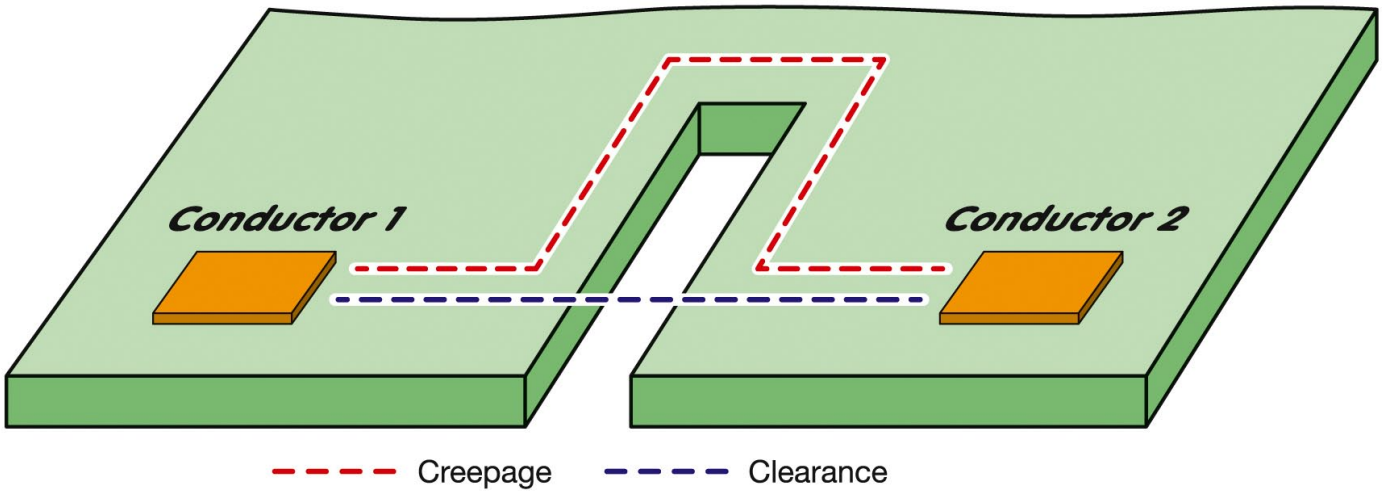


Figure 1. *A simplified representation of creepage and clearance distances.*

Creepage distance is the minimum distance between two conductive points when measured along the surface of the insulation. If creepage is not sufficient, then the possibility exists for a localised deterioration of insulating material to create a conduction path, which can lead to an unforeseen electric discharge.

For engineers who have designed in the medical environment, these terms will be very familiar, but now as we design equipment to be compliant for high altitude operation, these parameters are also more frequently encountered in other industry sectors.

One further consideration is the condition of the atmosphere that the power supply will be functioning in, and this is referred to as the Pollution Degree; the author concludes this explanation of 5000-m operating parameters with this topic – click the link.

Download PDF of Article

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10 MUST-HAVE DEVELOPMENT TOOLS THAT (MOSTLY) WON'T STRAIN THE BUDGET

JACOB BENINGO, FOR EDN

As an independent consultant, the advantage to having the right set of tools available for the job is only too apparent. Having the right tools not only decreases stress but also increases productivity and efficiency at a rate that far outweighs the cost of even the most expensive tools. After taking a few moments to consider the tools that make my job easier and more efficient, I've compiled a short list of 10 tool categories that are must-haves.

In forming this list, I have chosen tools that are relatively inexpensive but have made all the difference in my ability to produce value efficiently. The tools mentioned also are ones that I personally use and have no financial or developmental tie to. They are simply tools that I must have to get the job done.

Tool #1 – Top-notch Text Editor

Many IDEs come with a text editor that contains standard text editing features. These features may include basic search, replace, etc. These basic features are great for the hacker or maker whose 40-hour a week job isn't to develop embedded software. A professional embedded software engineer, though, needs a top-notch text editor with features beyond the basics. Features such as the ability to perform multi-selection editing, batch editing, and text transposition, to name a few, are features that give the professional an efficiency edge.

One of my favourite text editors to use is Sublime Text 3. The text editor is supported across multiple platforms such as Windows and Mac. Sublime Text is also free to try indefinitely with a friendly periodic reminder to purchase the tool for less than $100. One other feature I have found useful is that the development language can be specified, which then lets the tool perform keyword and syntax highlighting. In any event, the moral of the story is that a serious developer needs a high-end text editor beyond the capabilities of those included in your standard IDE distribution.

Tool #2 – Text Comparison Tool

Tools such as SVN and Git provide basic functionality for comparing the current version of a file or folder with its previous version. I have had times, though, when these basic tools just don't fit the bill. For example, on occasion I have updated source from a client or third-party vendor come across my desk that isn't revision controlled. I could add the code to my own revision system but for the most part I have no interest in having this third-party code in my system. In order to determine what has changed, I can use a tool such as Beyond Compare that can generate a change report so that I can see every change that has occurred in every file at a glance.

I have found at times, when a code base breaks and incremental compare and updates are necessary, Beyond Compare has worked wonders beyond anything that SVN or Git tools have to offer. The best part is that the 30-day trial is a literal 30-day trial. One day is a day that a developer opens and uses the tool and not just 30 calendar days since installation.

Tool #3 – Static Code Analyser

One of the most important tools that every embedded software developer should use is a static code analyser; a tool that performs an analysis on the software without running it and performs syntax checks on the code that go beyond the checks of a compiler. The static analyser can identify a large number of possible coding errors such as the lack of a default case in a switch statement, ambiguous code blocks, non-reachable code, and many other coding errors that result in difficult-to-find bugs.

Unfortunately, static code analysers tend to be

The Salea Logic 16 is an attached module to a PC or laptop.

pricey. The least expensive professional grade analyser runs around $500 with the most expensive being 10s of thousands of dollars. I personally have been using PC-Lint for years but when I have additional tools available I utilise them as well. A static analyser is an indispensable tool of an embedded software developer and it is critical that one is used.

Tool #4 – Code Metric Analysers

Monitoring from a metric standpoint the embedded software that is developed is just as important as designing and implementing the software. Tracking the number of lines developed and the complexity of the implemented code can be critical to identifying potential bugs. Metric tools can also monitor development progress that can then later be used to help develop models and estimates for the development of similar work. There are many such tools out on the market but one of my favourites that I use throughout the development cycle is the MSquared Resource Standard Metrics (RSM). RSM has a large number of metrics that can be generated and it produces reports in multiple formats that are simple and to the point.

Tool #5 – Logic Analyser

There are many different communication protocols that developers get to play with, such as UART, I²C, SPI, USB, etc. When problems arise on these communication channels or when drivers are being developed for external ICs, it is critical for the engineer to be able to see what is going on with the bus. For this reason it is imperative to have a really good logic analyser that can be used to spy on the bus. There are many great logic analysers out on the market. The logic analyser that I have been using for years that I have abused and used to the point that I've gotten every penny worth out of it is my Saleae Logic analyser.

Tool #6 – Communication Protocol Tools

The first step that I take when developing a driver with a device outside of the microcontroller is to mock up a development board and connect a communication tool to the device. For example, if there is an EEPROM device, rather than write an EEPROM driver first, I connect my Aardvark from TotalPhase and walk through the different commands that I would want to use. Using the communication tool, I can then send commands, watch the responses, and get a feel for how the device works before jumping into the guts of a driver. I've found that whenever I develop this way there are fewer mistakes and hurdles to jump

through to get the device up and running.

Tool #7 – Application Templates

Developers should be creating templates and processes related to the daily operations of their software development. Creating templates provides a way for developers to solve a problem once and then make it available to themselves and others again in the future. One example of a template that I mention far too often is a Doxygen template that I use for all my header and source modules. Rather than starting from scratch each time, when a new module is developed the template is copied in and modified for the new purpose. There are many different types of templates that can be developed. For example, hardware abstraction layer templates and driver design patterns can be templated amongst others.

Tool #8 – Development Kits

Development kits have proven to be a great way for developers to get up to speed quickly and also to test ideas and code before ever having to spend big money. Most general development kits now range from around $10 to $40 dollars. Developers can now afford purchase not just a single development kit to try out but instead have a large variety on the bench from which to run test code and experiments. I keep a wide range of development kits on my bench, ranging from ST Microelectronics STM32 Nucleo boards to Freescale Kinetis Freedom boards, just to name a few. I have a collection of different development kits offered by numerous vendors that allows experimentation and comparison so that the right part can be selected for the application.

Tool #9 – Energy Monitors

Monitoring the amount of energy that an embedded system consumes has become an important part of the design cycle. There are many ways to go about monitoring energy consumption, such as creating a home brew circuit or using an external tool. One method that I have found to be interesting is to use the IAR I-Jet and/or I-Scope. These tools have the ability to monitor currents and voltages that can then be correlated back to the function that was executing code. Correlating the current draw to the executing code then allows any high-energy consuming functions to be identified and optimised.

Tool #10 – Professional Compiler

Compilers tend to get a bad rap from developers. A compiler is probably one of the most important tools that any embedded software developer could have, yet, it is the tool that no one wants to pay for! Professional compilers range on the low end from around $500 up to the typical price of $1500, and usually have a free version for development up to around 32K of code space.
One commonly overlooked benefit of a professional compiler, beyond just the additional toolsets that are available as part of the IDE, are the optimisations. A professional compiler version is capable of applying optimisations that can squeeze the code space and RAM usage down. For a product that is shipping in even moderate volumes, such optimisations could allow for a smaller and cheaper part to be used. What could the potential cost savings be? The potential savings is most likely far more than the compiler's $1500 price tag.

There are many must-have tools that every developer needs in order to get the job done in timely manner. I have listed 10 categories of tools that have been indispensable in my embedded system development efforts and that are worth the investment cost. What development tools have you found to be useful during your own development efforts?

Jacob Beningo *is a Certified Software Development Professional (CSDP) whose expertise is in embedded software. He works with companies to decrease costs and time to market while maintaining a quality and robust product. Feel free to contact him at jacob@beningo.com, at his website www.beningo.com, and you can sign up for his monthly Embedded Bytes Newsletter.*

3D POWER PACKAGING: FOCUS ON EMBEDDED SUBSTRATE TECHNOLOGIES

By Brian Narveson and Ernie Parker, PSMA Packaging Committee

The power electronics industry and the semiconductor industry, inseparably intertwined with one another, are facing unprecedented efficiency, cost, construction and thermal challenges which provide many opportunities for innovation.

These industries are in the focal point of the "energy challenge" a multifaceted problem that involves mobile and cloud infrastructure systems, Internet-of-Things, renewable energy, smart grid, vehicle electrification, and across-the-board power efficiency enhancements in order to keep up with the IT industry's rapid growth in data consumption. These are the competitiveness and sustainability challenges of the twenty-first century.

The paradigm shift we have been experiencing in semiconductor packaging technology was brought about by advanced deep sub-micron semiconductor technology reaching a "cost barrier" that prevented further cost reduction by reducing transistor size and adding more functions to the semiconductor die. This barrier was circumvented through the development of wafer thinning that enabled through-silicon-via (TSV) technology, and the eventual introduction of 2.5D and 3D integration that facilitated heterogeneous ("More than Moore") integration. It will allow the power requirements of the digital load to increase 2 to 5 times, within the same footprint, in a single generation. The power sources community must now find ways to package power sources that will meet this demand, but with no increase in footprint.

In parallel, power semiconductor technology is facing a "construction barrier" that prevents realisation of the huge benefits new technology can offer in terms of increased power efficiency and higher power density. These new technologies include gallium-nitride (GaN), silicon-carbide (SiC), and gallium-arsenic (GaAs) power semiconductor devices that require operation in an environment that is free of bond wires and minimises parasitic interconnect elements. The leading packaging technology to achieve a significant reduction in parasitics (L, R, and C) is embedding active and passive components in printed circuit boards (PCBs) and using packaging technologies developed for 2.5D and 3D integration by the semiconductor industry, outsourced semiconductor assembly and test (OSAT) services, and original equipment manufacturers (OEMs). Thus existing 2.5D and 3D integration and component embedding becomes a key enabling technology for high density power sources utilising these new power semiconductor devices.

These multiple factors, led the Power Sources Manufacturing Association (PSMA) Packaging Committee to commission a power packaging study that would focus on 3D embedded technology for power packaging. PSMA commissioned LTEC Corporation to execute the study between May 2014 and February 2015. The 336 page report "Current Developments in 3D Packaging with Focus on Embedded Substrate Technologies" was derived from the research of over 740 published articles, interviews with 30 industry and academic experts, and attendance at 10 trade shows. The purpose was to determine the availability of embedded substrate technology usable today, and in the future, by the power industry.

The report is intended to assist executives and engineers in their own analysis of how currently-available materials and processes could be best used for the creation of advanced high efficiency, high power-density power sources. The report builds upon the findings of the Phase I report ("3D Power Packaging") executed by Tyndall National Institute and issued by the Power Sources Manufacturers Association (PSMA) Packaging Committee in 2014. This

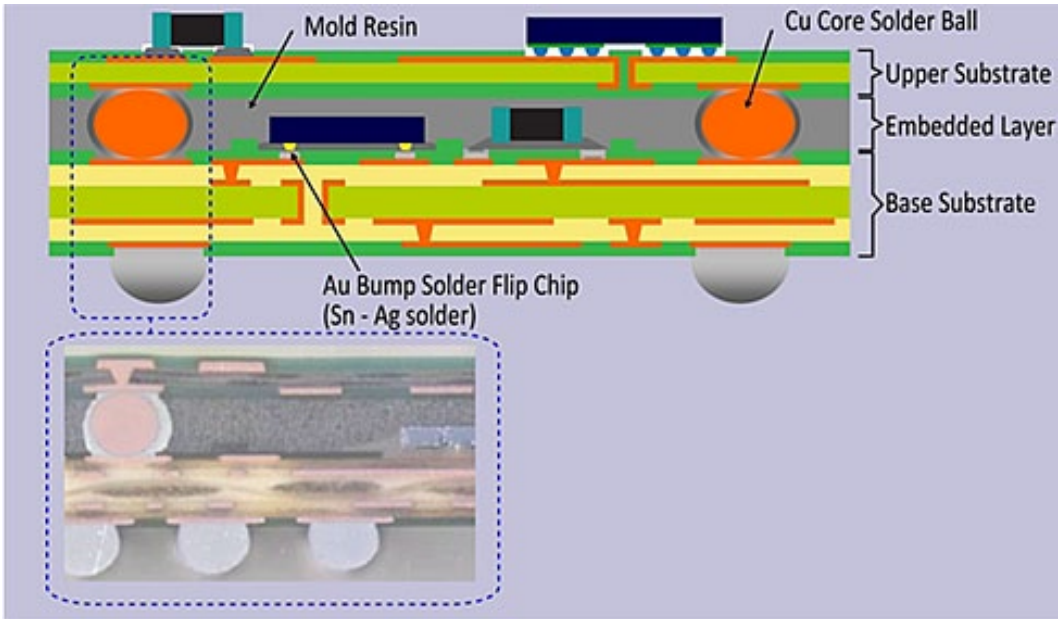


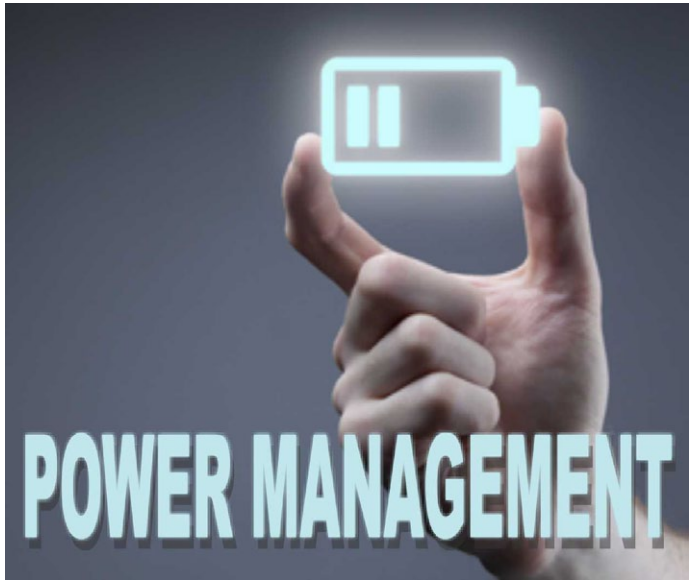
Figure 1. *Example of embedded substrate technology (Shinko MCEP)*

article will present the strategic observations and implications based on the findings of both reports.

For the purpose of this article the following definitions apply: Embedded substrate technology is defined as the inclusion of at least one active or passive electrical component within [between] the top and bottom conductive layers of a substrate, with a substrate defined as a planar structure having multiple conductive and insulating layers. A 3D Embedded Power Module is defined as a system that uses a combination of at least one controller/driver IC, at least one active component in the power train, and associated interconnect means, embedded in a single package, where the Z-axis is used to reduce footprint and increase power density.

Figure 1 provides an example of this technology based on Shinko Electric Industries Co.'s (Shinko) Molded Core embedded Package (MCEP) process.

As part of the project 30 companies were surveyed to determine why they were actively producing or developing power sources utilising embedded technology... *article continues, click the link.*



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DECIMATION FOR ADCS

BY IAN BEAVERS, ANALOG DEVICES

Wideband gigasample-per-second (GSPS) analogue-to-digital converters (ADCs) provide a wide frequency spectrum and many performance benefits to high-speed acquisition systems, but while some applications need a wideband front end, others also require the ability to filter and tune to a narrower band of spectrum.

It is inefficient for an ADC to consume the power necessary to sample, process, and transmit a wideband spectrum when only a narrow band is required. The FPGA transceivers previously required to decimate and filter the wideband data in subsequent processing can be eliminated as high-performance GSPS ADCs integrate digital down-conversion (DDC). This minimises the data rate and system layout complexity by lowering the number of JESD204B output lanes.

Decimation allows observation of a periodic portion of the ADC samples while ignoring the rest, which results in reducing the sample rate of the ADC. For example, decimate-by-M outputs the first M samples in each period, while discarding all the other samples in between M multiples.

The ADC must include a numerically controlled oscillator (NCO) and a filter-and-mixer component that are used as a companion to the decimation function. Digital filtering effectively removes the out-of-band noise from the narrowly defined bandwidth that is set by the decimation ratio. A digital tuning word to an NCO, used as a local oscillator, provides a fractional divider of the sample rate, with placement accuracy determined by the number of bits of resolution. The tuning word has the range and resolution to spectrally place the filter wherever it is needed.

The passband of the filter should match the effective frequency spectrum of the converter after the decimation. A distinct advantage of using DDCs is the ability to position the harmonics of the fundamental signal such that they fall outside the band of interest.

Digital filtering by the DDC filters the noise outside of a smaller bandwidth. The SNR calculation of an ideal ADC must account for the processing gain of the filtered noise. Using a perfect digital filter, the processing gain due to the filtered noise will increase by 3 dB for every power-of-two reduction in bandwidth:

Ideal SNR (with processing gain) =
6.02 × N + 1.76 dB + 10 × log(fS/(2 × BW))

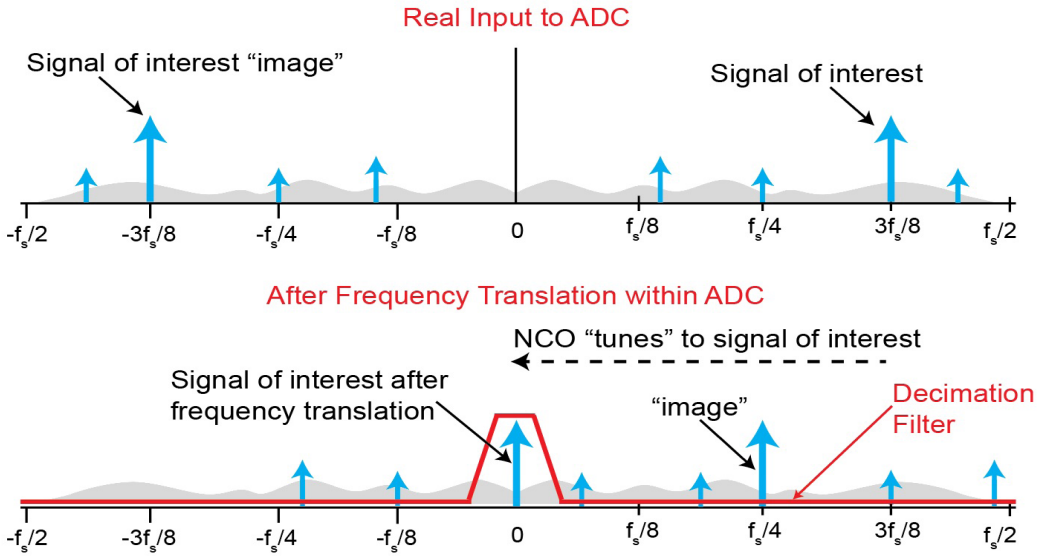
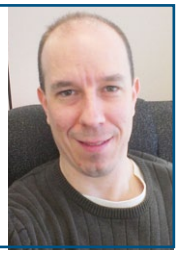


Figure 1. *Frequency translation using a low-pass filter and NCO achieves a bandpass filter. Frequency planning ensures that unwanted harmonics and spurs fall out of band.*

Ian Beavers *[ian.beavers@analog.com], a staff engineer for the Digital Video Processing Group at Analog Devices (Greensboro, NC), is a team leader for HDMI and other video interface products. With over 15 years' experience in the semiconductor industry, he has worked for ADI since 1999. He holds a bachelor's degree in electrical engineering from North Carolina State University and an MBA from the University of North Carolina at Greensboro.*



Spin Cycle

High-performance motor control at low speeds

By Chris Clearman, Texas instruments

Sensorless motor control has primarily been used in applications where the majority of the operating time is at higher electrical frequencies (mechanical speeds). This is due primarily to the fact that most sensorless techniques require a back-EMF (Bemf) signal that is generated by the rotor's rotation at a minimum frequency. Being able to continuously estimate the rotor flux angle at zero and very low speeds and stably move between low-speed and high-speed estimators can improve the effectiveness of sensorless startup under load.

If you are a frequent reader of the Spin Cycle column, you may be aware of TI's FAST software observer used in the InstaSPIN-FOC software. FAST's minimum frequency of operation is much lower than that of other observers, sometimes below 1 Hz. But it still requires a minimum frequency.

Figure 1 *Frequency of operation for FAST software observer*

With sensorless techniques such as FAST, the initial rotor flux angle is unknown and, until enough Bemf is measured so that the algorithm can start estimating correctly, the estimates are unpredictable. But this estimated angle – even though incorrect – will be feeding the control system that will be applied to the motor and that may induce rotor movement. With just a small amount of rotor movement, though, enough Bemf voltage is produced so that the algorithm can converge on a reasonable angle estimate, allowing controlled high-torque drive into an area of excellent operation. So if enough torque is generated for rotor movement, this method can be used to start the motor, but it may not be consistent in start-up performance.

Generating enough torque

As the starting load is increased, the torque you can generate will be based on the current and the alignment of the fields (determined by the accuracy of the angle estimate). To ensure you can generate enough cur-

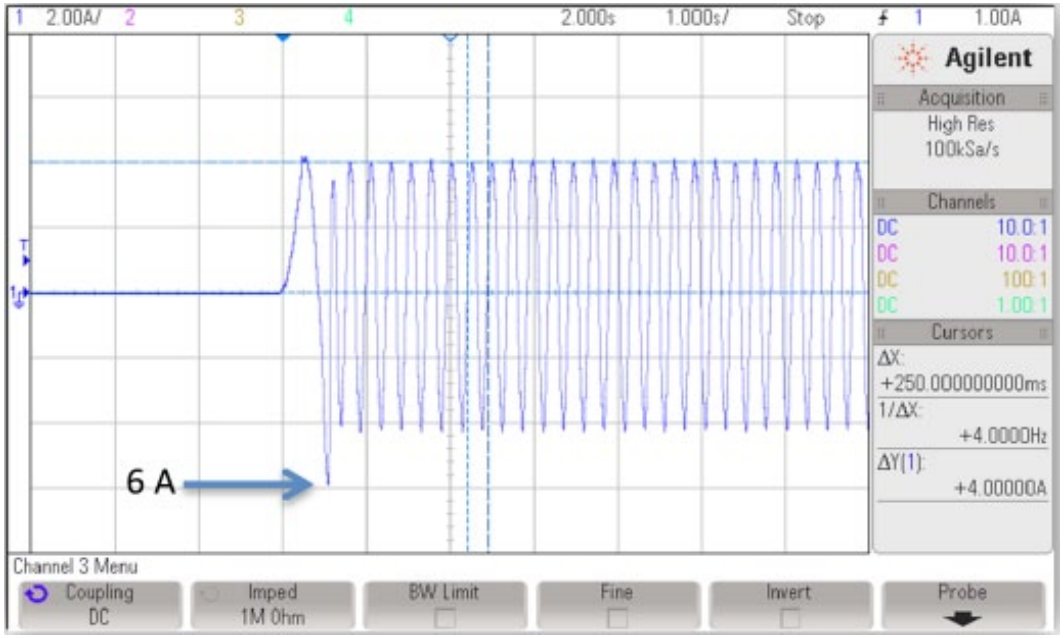


Figure 2 *Full load (4A continuous / 6A peak) start-up*

Spin Cycle

rent, it is imperative that the speed controller's maximum (positive and negative) output be larger than the rated current that is required to generate the rated torque. In the example in Figure 2, note the below waveform captured when starting a motor under full load. Producing the torque required to move this rated load requires 4A of current. In this case, the speed controller's maximum output was set to (6.0), and you can see that this 6A current was reached in the first electrical cycle to move the rotor. In this example, FAST was able to provide a valid angle, which allowed the control system to regulate the current usage immediately to only the required 4A.

Even though you are generating a stable feedback angle, that angle is not necessarily aligned properly to generate maximum torque. You are basically just sweeping a stator field and waiting for the rotor field to lock on and synchronise. When the stator field is not properly oriented, you will not produce enough torque or, in the worst case, produce torque in the opposite direction required. Improving this situation requires a better starting angle for the control system. But how do we do this when most sensorless control algorithms, including FAST, can't provide a valid angle at zero speed?

One way to do initial alignment in a field-oriented control (FOC) system is to inject a DC current into the Id portion of the control system (none into Iq). This is the D-axis, which is defined as the orientation of the rotor flux.

If this current is large enough to move the rotor (and any load), the injection will result in the rotor now being at a known angle (0 radians), meaning that while the forced angle is still emulated, it is at least starting in the proper orientation and in the best position to produce torque. This injection of DC current can be done "manually," or you can take advantage of the RsRecalibration flag included in TI's InstaSPIN-FOC solution.

Complete article, here

- click the link for the continuation of this column.

WHY FEC PLAYS NICE WITH DFE

BY RANSOM STEPHENS

At data rates above about 10 Gbits/sec, the frequency response and impedance mismatches from the transmitting end of one SERDES (serialiser-deserialiser) to the receiving end of another SERDES causes eye-closing ISI (inter-symbol interference). The combination of pre/de-emphasis at the transmitter and equalisation at the receiver fixes enough of that ISI to reopen the eye so it can operate at a reasonable BER (bit error ratio).

The receiver usually employs two types of equalisation: CTLE (continuous time linear equalisation) at its input and DFE (decision feedback equalisation) that feeds back ISI corrections following identification of 1s and 0s by the decision circuit.

The gross character of the channel (Figure 1), whether it's a trace between chips, traces from circuit to backplane to circuit, a module-to-host kind of thing, or cables, has the frequency response of a really bad low-pass filter. Correcting the response of a low-pass filter is easy: either crank up the high frequency components of the signal (pre-emphasis), attenuate the low frequency components (de-emphasis, strictly speaking), or both (CTLE and de-emphasis in real life).

DFE, on the other hand, corrects ISI by messing around with logic values rather than voltage levels so its frequency response is more or less flat.

Crank up the high frequencies

Murphy's Law (a.k.a., Sod's Law) guarantees that whatever you do to fix ISI will aggravate something else. If the most obvious effect of the solution is to amplify high frequencies, then that something else is likely to be crosstalk. After all, the crosstalk picked up by a victim is proportional to the slope of the aggressor's edge and that's all high-frequency content.

The hopeful, optimistic, naïve, soon-to-be unemployed engineer will point out that differential signalling has protected us from both generation and reception of crosstalk for years. But in the neighbourhood of 10 Gbits/sec, bit periods and rise/fall times drop so low that differential skew and non-zero trace separation let aggressors transmit crosstalk and can't prevent victims from absorbing it. Too bad.

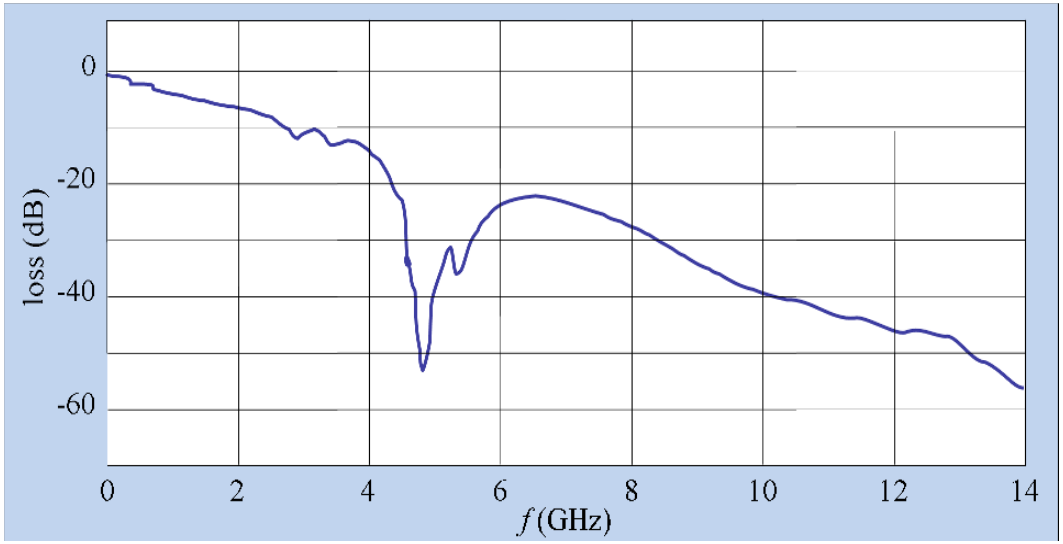


Figure 1. *"Typical" channel frequency response (source, Ransom's Notes).*

Even though it's crosstalk agnostic, the real trouble comes from DFE. Left alone, pre/de-emphasis and CTLE would amplify crosstalk's high frequencies and the detector would experience a few errored bits, but when combined with DFE, Murphy and Sod conspire to cause burst errors: enter FEC.

FEC (forward error correction) is mathematical magic. At the transmitter, you take a bunch of data bits, add a few extra parity bits—

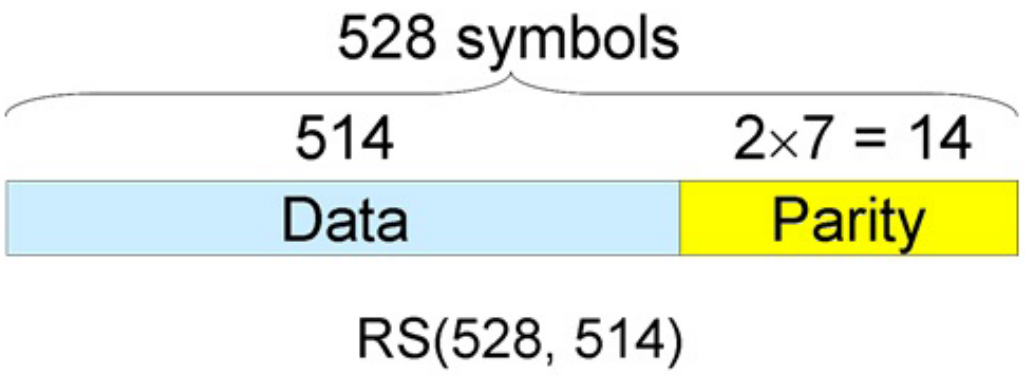


Figure 2. *Reed-Solomon forward error correction (source: Ransom's Notes).*

really a generalisation of parity or CRC (cyclic redundancy check) bits—and run the whole "frame" through a well-chosen binary polynomial. At the other end, you run the received frame through the inverse of the polynomial, wave a logical wand, and, voila! You both identify and correct some bit errors. There are restrictions, of course, it's only magic until it fails.

100 Gigabit Ethernet and OIF-CEI use Reed-Solomon FEC (forward-error correction) coding, RS(528, 514). First, let's think in terms of generic symbols, we'll convert back to bits in a second. The idea of RS(528, 514) is that you encode 514 data symbols and 14 parity symbols into a 528 symbol frame (Figure 2). The coding-decoding process can correct up to 7 errored symbols.

Now, back to bits. 100 GbE uses 10-bit symbols. So the 528 symbol frame is 5280 bits long, holds 5140 data bits, and employs 140 parity bits. RS-FEC can correct up to 7 symbols, no matter how many bit errors there are in each symbol. Let's look at a few cases:

At its most effective, RS-FEC can correct as many as 70 errors in 5280 bits provided that those errors come in very well placed strings of 10 in a row. That is, the errors have to fit perfectly in each of seven 10 bit symbols. At the other extreme, RS-FEC can always correct at least 7 bits, but if 8 bit errors are distributed across 8 different 10 bit symbols, RS-FEC won't be able to fix them. The statistics get messy.

Back to DFE and crosstalk

The "decision feedback" property of DFE means that it corrects ISI by assuming that each incoming bit has been interpreted correctly; it's called the "ideal decision" assumption and leads to DFE's Achilles' Heel: burst errors.

If we lived in an ideal crosstalk-cancelling differential-signalling world, the DFE might never see an error. After all, it's protected by both pre/de-emphasis and CTLE. Instead, those very protectors ratchet up the crosstalk stress, increasing the probability of an error.

When the decision circuit gets a bit wrong, the ideal decision assumption fails, and the DFE feeds back the wrong signal. That is, instead of cancelling out ISI, the DFE gives the decision circuit more noise and it's likely to generate another bit error. The DFE is then even farther out of control and burst or avalanche errors are likely to occur.

But RS-FEC loves burst errors! By encoding data into symbols and then correcting the symbols, RS(528-514) can correct a burst of up to 70 consecutive errors. Of course, the burst isn't likely to be organised to align in the symbol boundaries perfectly, but for an isolated burst, RS(528, 514) can stomach at least 61 consecutive errors.

After all the statistics have settled, the physical layer compliance test requires BER <5.0E-5 prior to FEC to assure a functional BER <1 E-15.

For the measly price of 14/528 = 2.65% extra bandwidth, you get a dramatically increased BER test budget. Cheap!

5 SECURITY DESIGN QUESTIONS YOU MUST ASK NOW

By Gregory Rudy, Green Hills Software

As cyberattacks on networks continue to grow dramatically, protecting your embedded devices has never been more vital. As connectivity increases, so does the threat of compromise and data breach. Such compromises result in the loss of intellectual property and reliability. Reliability is especially critical in embedded devices where end users trust, often times with their lives, that hardware and software is operating as designed.

For years device manufacturers have been following processes to assure production of high quality devices, traditionally focused on functional and environmental testing. Due to increased network connectivity, these same devices are now exposed to rigorous attacks, impossible to entirely replicate in a test environment.

If recent headlines have taught us anything, it's that IT networks cannot be trusted. Devices are no longer safe behind company firewalls, and as a result, security designs must now address the real threat of attackers having unrestricted access to device interfaces.

Designing for security involves the effort of multiple departments within an organisation and must be championed by management. In an effort to help managers assess the quality of their security design, following are five questions that every manufacturer should ask and answer today.

Question 1: Does your device refuse unauthentic commands?

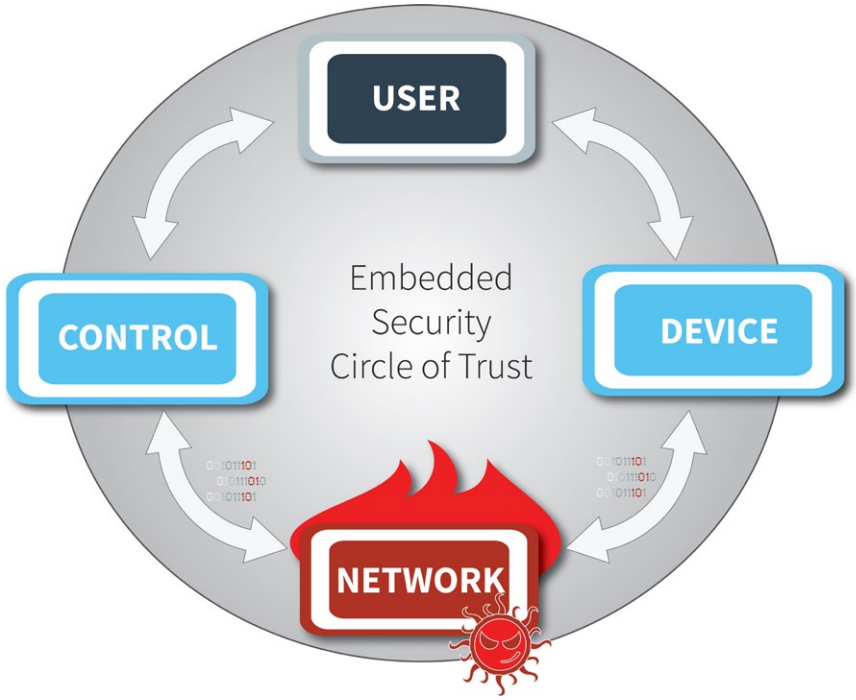


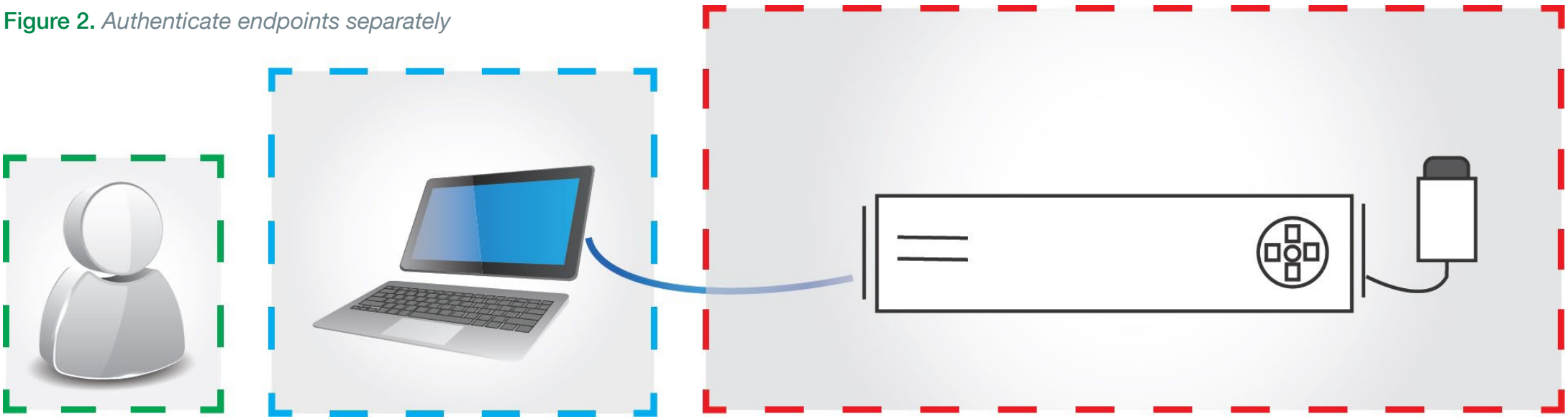
Figure 1. *Don't trust the network*

There are two methods attackers use to gain access to local networks: (1) Gain access to an information system already on the network, and (2) Tap into the physical network link itself. In either case, attackers can view data packets transmitting across the network link and reverse engineer protocols for malicious purposes.

Compromises are prevented by first identifying all end-points, including the device itself, control systems, user, and any other IT system receiving data. Control software should ONLY send commands after authenticating communication with the proper device, while devices should ONLY accept commands after authenticating the user. Vulnerabilities occur when a device grants access to resources without properly authenticating the end-point. Security designs should never assume valid users or control software just because the received commands are properly formed.

A good example is the publicised hack of network-enabled infusion pumps. Pump software assumed that any commands received

Figure 2. *Authenticate endpoints separately*



were from a valid source. Attackers gained access to the network link to reverse engineer the protocol and spoof the control application to send commands causing the potential to administer lethal doses to a patient.

Question 2: Can your device detect if it has been tampered with?

There are a number of ways malware can be injected into an embedded device:
- Re-programming through a hardware debug interface such as JTAG
- Unused, test, and debug interfaces left open, such as Telnet and FTP
- Code injection attacks of valid control interfaces developed using poor secure coding standards
- Software update that assumes trustworthiness without verification

Physical protection, vulnerability scanning, and penetration testing help prevent software tampering, but still cannot detect tampered software after it has occurred. The process of secure boot verifies the source and integrity of software using digital signatures. Software is signed during release and verified by the device prior to each execution.

When generating digital signatures for secure boot, it is important to understand that this is done in an out-of-band process. As a result, protecting private signing keys is critical. If an attacker was to ever obtain access to these keys, then security of ALL devices is vulnerable.

The author continues with Questions 3, 4 and 5 before sketching out a current-best-practice solution. Click the link for the pdf.

DON'T BURDEN YOUR INTERNET OF THINGS CONCEPT WITH HIGH MOBILE DATA CHARGES

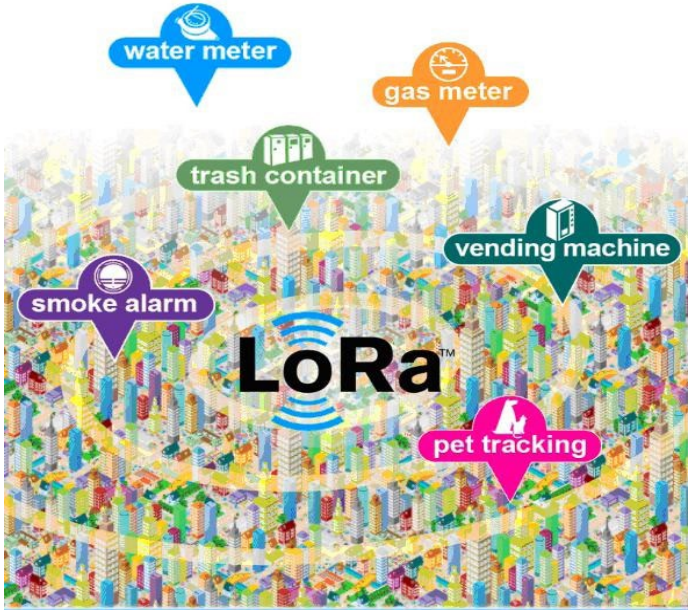
By Kevin Price, Future Connectivity Solutions

The vision for the Internet of Things (IoT) sees billions of devices connected to the internet, each with its own IP address. A connection to the universal network enables even the simplest of devices, such as sensors in a factory or LED lights in a home, to continually upload small bursts of state data in real time, and to act on commands sent by a remote controller.

The technology to accomplish this exists today. The IPv6 protocol supports a practically unlimited number of individual IP addresses. And through wired and wireless communications, a connection to the internet can be made in almost every inhabited place on the planet, and in many that are not inhabited.

One barrier to the realisation of this vision, however, has so far received too little consideration: the economic model for connecting wire-free, mobile or hard-to-reach devices to an internet access point. While mobile telephone network coverage might be almost universal in the industrialised world, a mobile data service plan comes at a high price. That's fine for expensively employed humans such as sales people or field service technicians, and for expensive assets such as shipping containers.

But for millions or billions of tiny devices such as sensors or actuators? Today, the cost of a mobile telephone connection is totally out of proportion with the cost of the device. And



that is why device OEMs should take note of a proven new technology for wide-area wireless networking, and ensure that new device designs are able to take advantage of the much cheaper connectivity option which is set to be available within the next 24 months.

The high cost of service plans

The internet is transport-neutral. A device may connect via a wired Ethernet network in an office, a Wi-Fi access point in a home, or through a mobile telephone mast from a farmer's field: the internet treats them all equally.

In a wireless sensor network or similar IoT application, therefore, users will normally want to choose the lowest-cost, feasible, means of connection. This will normally be a Wi-Fi or ZigBee (wireless) or Ethernet (wired) connection where available. But these are not available to remote or mobile devices, which today rely on a mobile telephone network to provide access to the internet.

But when a typical cellular telephone data service plan costs some $25 per month per device, the financial model for wireless sensor networks might not add up. In fact, the situation promises to only get worse, as Mobile Network Operators (MNOs) are keen to switch off their legacy '2G' GSM networks. Consumer demand drives the business strategies of the MNOs, and this demand is for very high download rates to support video streaming, file sharing, photo sharing and other popular applica-

tions. So MNOs are pouring investment into the roll-out of '4G' LTE networks, which offer wide-area mobile broadband capability.

By contrast, the old 2G networks offer far less attractive revenue opportunities: MNOs would prefer to eliminate the cost of maintaining and operating old 2G equipment and carry all data traffic on the newer 3G and 4G networks. But the higher data-rate service plans available on 3G and 4G networks are even more expensive than the basic offerings, putting mobile telephone airtime even further out of the reach of wireless sensor networks.

Today, then, some device manufacturers are tending to implement a compromised version of the IoT. In a gateway architecture, remote or wire-free devices connect wirelessly to a fixed gateway. The connection to the gateway may be via a technology such as Wi-Fi, Bluetooth Low Energy or ZigBee: licence-free, and with no airtime cost.

The gateway may have a fixed line link to the internet, or it may require a mobile telephone connection to access the internet, but in this case the high service plan cost is shared among the tens or hundreds of devices which might use the gateway.

This architecture may be suitable for some applications, but it has its drawbacks. The chief one is the limited range of the link between the node and the gateway: Wi-Fi, Bluetooth Low Energy and ZigBee all have a limited point-to-point range of typically less than 100m. A complex mesh network topology, which is supported by the ZigBee protocol, might be able to extend this to some extent, but only if one node is never more than 100m from another node.

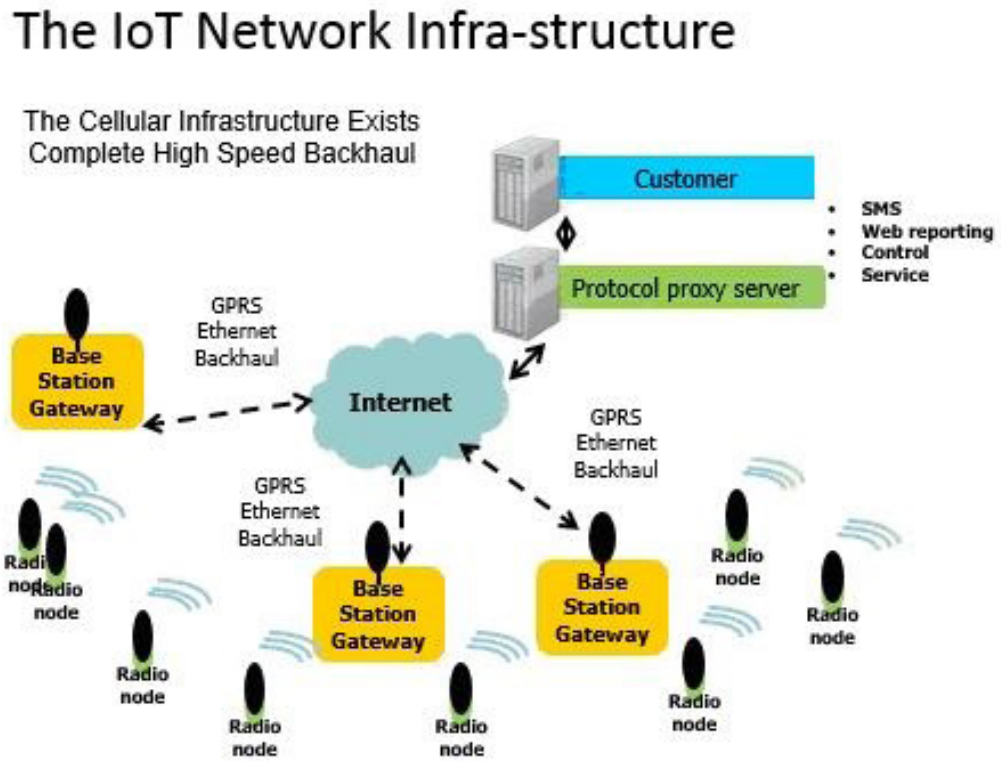


Figure 1. *devices with a direct connection to the internet via mobile phone masts can roam more widely than those tied to a local, private gateway*

Applications in which nodes are widely distributed or mobile over a wide area, therefore, cannot rely on this gateway architecture. They need their own, dedicated, long-range link to internet access points. And today, this is normally provided by a GSM module interfaced to a mobile telephone network (see Figure 1). However, an attractive alternative is emerging.... *click the link for the continuation of this article.*

THE SEVEN LEVELS OF IP VERIFICATION

By K Charles Janac, Arteris

The quality of semiconductor intellectual property (IP) is a major issue for design teams utilising third-party sources for portions of their SoCs. Quality is even more critical for highly configurable types of IP because customers license it specifically to address the unique requirements of their systems and markets. The on-chip interconnect fabric is perhaps the most common example of highly configurable IP, and its quality is paramount to enable first-pass success for SoC creation.

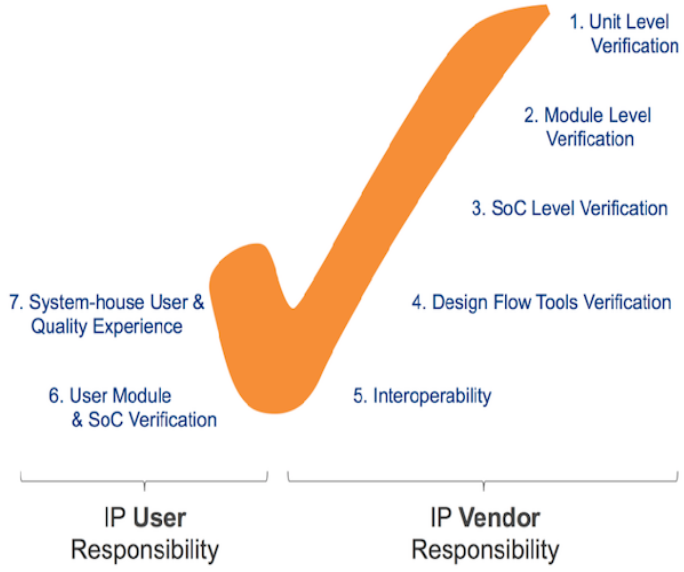


Figure 1. *The process of identifying IP quality is long and arduous, and most of the responsibility falls on the vendor.*

Thorough verification is critical because the initial cost of configurability pales in comparison to the cost of slowing down a tapeout. Configurability enables customers to innovate in an infinite number of ways; however, its use also makes corner case verification extremely important.

To obtain sufficient quality, it is critical to use a configurable IP that has been proven in production SoC designs. If it has been implemented in large volume SoCs and has been verified at multiple design and production levels, then it has "proven" configurability. But even at this level, every customer makes certain risk tradeoffs for new IP – Do they want the most advanced features to address a new market? Do they want something proven and less risky? How to decide?

Trust but verify: introducing the 7 levels

If your team wants to assume the least amount of risk and get to market promptly, then it has to evaluate an IP candidate on seven levels of verification. If a user wants to feel more comfortable with quality throughout the entire SoC life cycle, then the IP must pass all seven levels of verification described here:

Unit-level - For units and elements that make up the configurable IP, this foundational level is critical to the process because bugs or issues found here will result in problems at subsequent levels.

Module-level – This is generated in the actual user configuration that will be implemented in the SoC based on required performance parameters and topology. At this level, the configurable IP mates with the functionality of others in the design. It should be verified by the vendor first, and should be based on representative design examples and results should be made readily available to customers.

SoC-level – The IP vendor should verify representative customer configurations using a number of sample SoC designs - ideally, provided by customers - to verify performance and quality. This includes release-to-release design performance drift verification.

Design flow tool verification – This includes testing of any tools used to configure and generate the IP, whether the tool suite is controlled by the command-line, a graphical user interface (GUI), or both.

Interoperability – The IP vendor needs to demonstrate testing results for transaction and communication protocols such as AMBA and customer proprietary protocols. Also, EDA tool and verification IP integrations with key partners should be demonstrated.

Customer module and SoC verification – Occurs during the design, tapeout, bring up and debug phases. The customer should be able to implement, integrate and verify the customer-configured IP at the same or higher confidence as if it were hand-coded by an internal team.

Customer, system-level user and quality experience – Includes system house and end-customer system lifecycle testing.

The most important parts of the verification sequence are the last two customer phases. Here, it is critical that an IP company possess the people, culture, processes and execution in its internal verification program to not only ensure that the IP vendor delivers quality IP, but also enables customers to easily verify their own custom configurations of the IP. This is a long-term process and requires a relationship of trust between the IP vendor and user, because although users can perform all varieties of testing and verification, until they successfully deploy the IP in sufficient volume they won't know what problems will be encountered. Anticipation and analysis does not equal first-hand knowledge. This is why vendors that have design wins for a narrow set of target applications often encounter deployment problems outside of their originally targeted market space.

Quality takes time

Because initial price of the configurability is relatively small compared to the potential impact on SoC delivery, it is essential to deliver proof in processes, procedures, time and experience to ensure customer confidence. Additionally, the technical benefits of anything new must far outweigh the potential risks to function, quality and delivery schedule. These are the main reasons why it takes about 10 years to build a strong IP company: The provider not only has to build the product but also must get it designed into a sufficiently broad set of applications. Then the customer must successfully deliver the SoC and have system houses incorporate the chips. Finally, the customer has to deliver sufficient volumes to prove that the quality has a positive impact on its system-house business. Only then can the value of quality be correctly quantified.

In this process, IP vendors have to keep up with major technology changes and specific customer requests while maintaining strong support and impeccable quality. This is not easy to accomplish. As a result, successful [IP] companies such as ARM, Synopsys, Imagination, Tensilica (Cadence), and Arteris were not built quickly. That's because it takes time for the product to achieve the seven levels of verification and production volume success.

Commercial vs. Internal development

Achieving these verification levels requires the configurable IP vendor to experience a broad range of SoC designs implemented into a variety of systems, which ideally results in a higher quality product than is possible to develop internally. Quality at this level is difficult for internal interconnect groups, in all but the largest semiconductor companies, to attain; because internal teams see a relatively small number of designs and a relatively narrow variety of design methodologies.

A rule of thumb: The greater diversity and number of successful system design-ins, the greater the quality and ultimately the value of configurability.

Interoperability and ecosystems

A configurable IP is just one of hundreds of components and subsystems that make up an entire SoC. Therefore, the ecosystem around

it is quite important. Interfaces to others must be tested and interoperability must be assured. In particular, ARM's AMBA standards have emerged as being the most widely adopted, therefore it is very important for vendors to monitor and implement the stream of ARM standard developments in order to assure trouble-free customer integration.

Customers also use a variety of EDA tools and methodologies that have to be tested with configurable IP to assure smooth interoperability. Customers want to focus on design, and don't need to be sidetracked with interoperability problems. Ecosystem testing and verification is in the best interest of all involved as seamless integration accelerates use of all IP involved. The vendor needs to complete this early in the process before interoperability issues start hitting development schedules.

Quality makes commercial IP possible

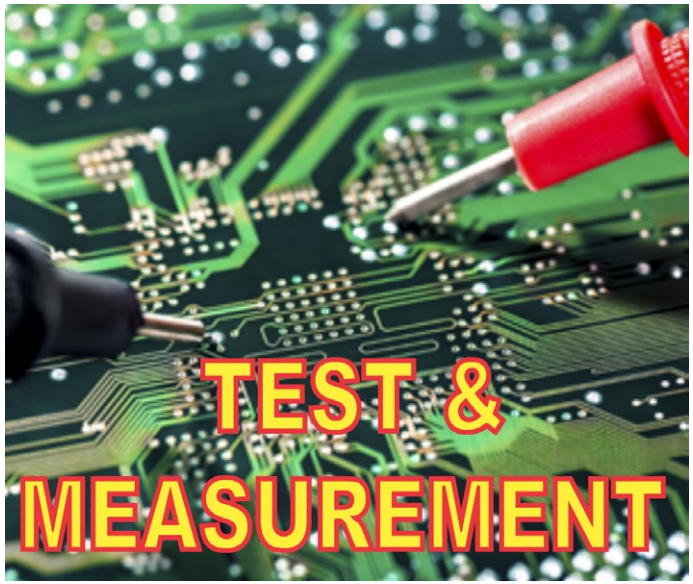
Of course, verification and quality of are not the only considerations for adoption. New technologies and standards emerge all the time and configurability has to support this continuous evolution. Innovations that improve quality of results and productivity must also translate into reduced SoC costs. Therefore, the selection of IP involves a trade-off between technology benefits, cost reductions and quality risk.

If the technology benefit is high enough, the quality risk will be worth taking. For example, low-power processor cores, configurable processors, high performance GPUs, and network-on-chip interconnects were once unproven technologies developed and marketed by small companies. Today, they are proven in some of the most complex SoCs ever made, leading to a virtuous cycle of greater customer comfort and adoption, superior quality, and higher technological investment and innovation. The secret is that all these technologies evolved through solid quality programs and global support organisations.

A quality electronic system, made up of quality SoCs, needs to be made of fully verified components. It is vital for chip designers then to scrutinise any candidate IP with the seven levels of IP verification to warrant consideration.

Charles Janac *is Chairman, President and CEO of Arteris, where he is responsible for establishing and growing a strong global presence for the pioneer of NoC technology.*

Find SOC IP on EETsearch



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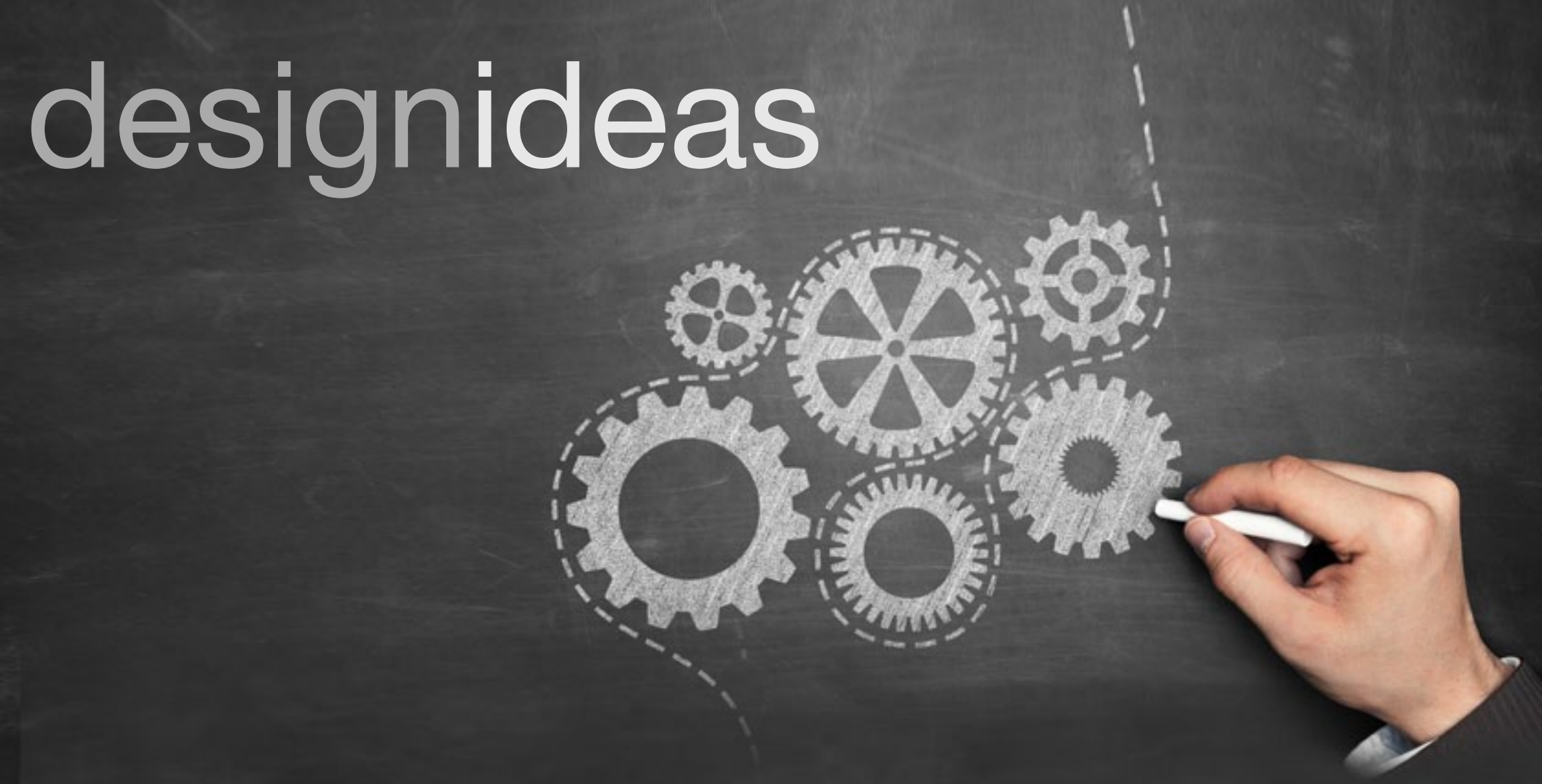


- Simplified kurtosis computation detects signal interference
- Simulate digital filters with PSpice

Simplified kurtosis computation detects signal interference

By Kaushal Buch

Kurtosis, or the fourth central moment in statistics, is commonly used to estimate the shape of the statistical distribution of a signal (or data). It is widely used for detecting non-normality in the signal received by communication receivers used in digital communication systems, passive microwave radiometry, time-series analysis, image processing, and radio astronomy, to name a few. It also finds application in detecting energy and power in certain modulation schemes and in measuring inter-system interference for communication systems. In most of the cases, Kurtosis is primarily used to detect the presence of strong man-made radio frequency interference which contaminates the distribution and makes it non-normal. Kurtosis is calculated as shown in Equation 1.

$$K = \frac{\Sigma(X-\mu)^4}{(\Sigma(X-\mu)^2)^2} \qquad (1)$$

where:
K is the kurtosis value
X is the input data
μ is the mean of the N samples considered for the computation
∑ represents the average

In the case of a normal (Gaussian) distribution, the Kurtosis is 3. Since we are calculating Kurtosis for a finite number of samples, the estimated value would have some uncertainty defined by the estimation error, and hence for the normal distribution, the value would be 3 ± δ (the estimation error). Thus, for a given input data set to be considered normally distributed, the value of Kurtosis must lie within these limits.

Computation of Kurtosis on an FPGA or other DSP platform is computationally intensive, primarily because it needs a division operation. This Design Idea avoids the division altogether, and uses two multipliers and other blocks to determine whether the input data passes the Kurtosis test. This approach utilises the fact that in order to check the normality of the distribution, it is only required to determine whether the Kurtosis value falls within defined limits. The conventional method for calculating Kurtosis involves division, as shown in Equation 2.

$$K+\delta > \frac{\Sigma(X-\mu)^4}{(\Sigma(X-\mu)^2)^2} > K-\delta \qquad (2)$$

Rewriting Equation 2 to avoid division requires two multipliers, as shown in Equation 3. The comparators are required in either case.

$$(K+\delta)*(\Sigma(X-\mu)^2)^2 > \Sigma(X-\mu)^4 > (K-\delta)*(\Sigma(X-\mu)^2)^2 \qquad (3)$$

The elimination of the division operation leads to significant resource savings on an FPGA. In the case of an 8-bit input, the division has to be carried out on a greater-than-16-bit dividend and divisor. This is because the computation requires multiple squaring and accumulation operations, each of which leads to bit growth. The elimination of division also makes single-cycle throughput relatively simple to implement. These features make the technique amenable to integration in real-time signal processing systems, particularly for area and timing constrained designs. The block diagram for the design described by Equation 3 is as shown in Figure 1.

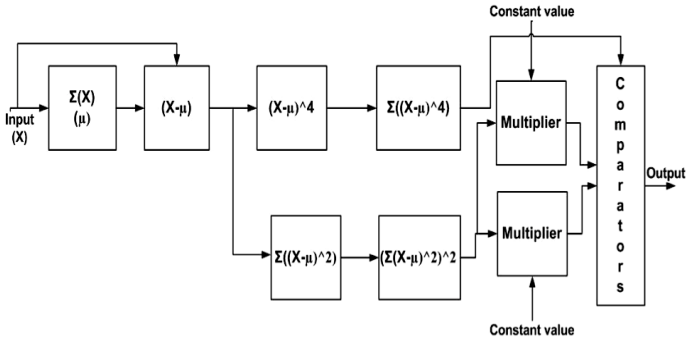


Figure 1. *Block diagram of the design*

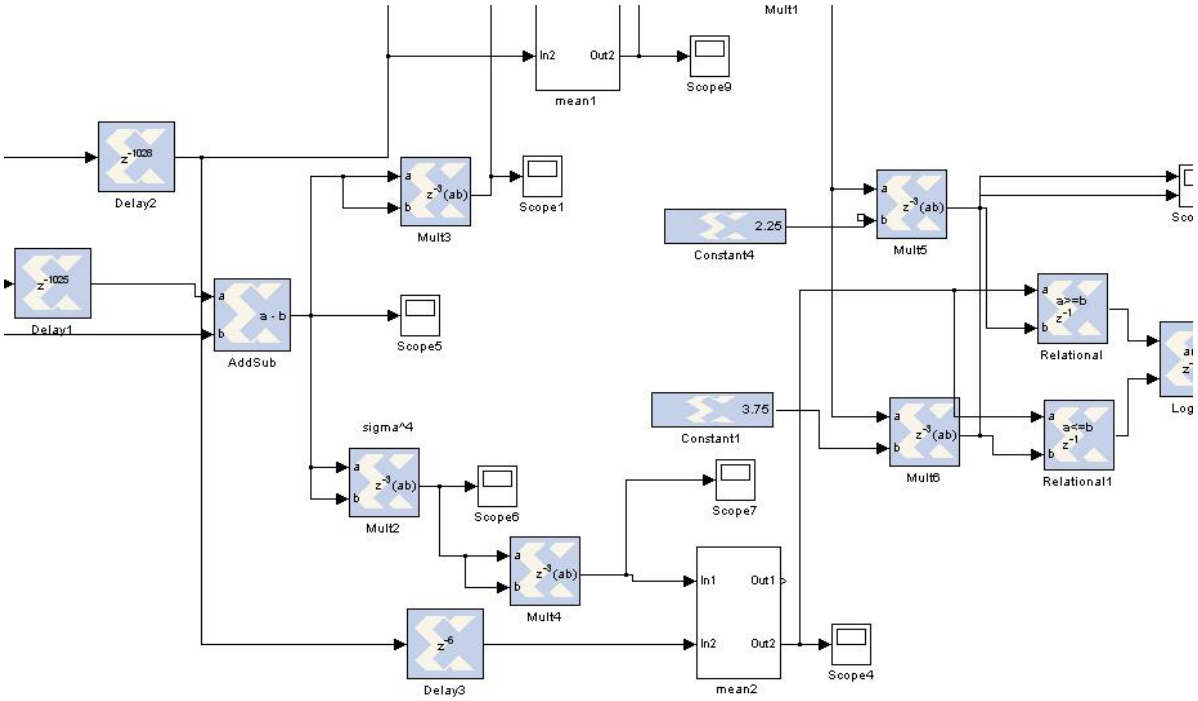


Figure 1. *View of the Kurtosis design made using Xilinx System Generator*

This idea can be extended to finding abnormalities in distributions other than the normal distribution by changing the expected value of K and δ if the window size changes.

The design was tested on a Xilinx FPGA by providing digital samples of an 8-bit pure Gaussian signal, a Gaussian signal with impulse interference, and a sinusoidal signal. The design was created using Xilinx System Generator and uses about 2% of the hardware resources on a Virtex-5 FPGA for 8-bit data having a window size of 1024 samples. The design has been tested up to a 250 MHz clock frequency. A design using a divider would require about 8-10% of the FPGA, and would increase the latency of the Kurtosis computation.

Referencing Figure 2: the multiplier blocks are used as fixed point, and one inputs of each is a constant (the estimation errors). The delay added in the multiplier block is shown by the z-3 parameter, indicating three clock cycles, which is added to meet the timing requirements. The multipliers are followed by a set of comparators to check that the Kurtosis is within the prescribed limits. The comparison outputs are ANDed to get the final output. A value of '1' at the output indicates that the input distribution is Gaussian, and a '0' indicates otherwise.

A design file is available to download.

Although the design was tested in an FPGA-based real-time system as a detector for removal of samples corrupted by interference, it is also effective for implementing a software-based Kurtosis test.

Applications of Kurtosis computation in the field of digital signal processing and digital communication are:

- Removal of radio frequency interference in data received by highly sensitive communications receivers of passive microwave radiometer. Used in satellite payloads to remove pulsed interference and modulated interference from the received signal.
- Mitigation of radio frequency interference to improve the sensitivity of radio telescope receivers. It is useful to remove time and frequency domain impulsive interference due to power-line sparking, automobiles, communication transmitters, etc.
- Detection and removal of non-normality due to impulsive interference in time and spectral domain signal.
- Finding the statistical distribution of the received signal in digital communication receivers. This helps in testing receiver performance in the presence of interference.
- Energy and power detection in on-off keying based modulation, useful for certain ultra-wideband systems.
- Measurement of intersystem interference.

Simulate digital filters with PSpice

By Dobromir Dobrev

PSpice has become an industry standard tool for analogue circuit simulations. Analogue circuits have real physical realisations and can be simulated with their schematic representation, and the frequency response is a consequence of the circuit time constants. In contrast, digital filters perform mathematical operations on a sequence of samples. The digital filter's time constants are hidden in the sampling interval T. So, digital filters are usually simulated only mathematically by their transfer functions, and to do this, it is important to have an easy way of simulating the sampling delay $T=1/f_s$, introduced by the sampling rate f_s, because this delay defines and scales the overall filter response.

Usually, the Laplace transform is used for behaviour modelling of analogue circuits because it transforms the time domain into the complex frequency s-domain. The frequency response of a digital filter serves a particular case, and can be derived from the Time-shift theorem (Delay theorem) of the Laplace transform. The theorem states that, if a time function f(t) is delayed by a time T in the time domain, the result in the frequency domain is a multiplication by e^{-sT}, see Eq. (1).

The term e^{sT} is often referred to as a delay operator, and if it is replaced by the symbol z, as in Eq. (2), the Laplace transform rises to the so called z-transform. Thus, coming back to the time domain, z^{-n} corresponds to the delayed nth sample, z^0 is the current sample, and z^n denotes the future nth sample.

$$z^n = e^{nsT} \qquad (2)$$

This Design Idea presents a fast, simple, and intuitive approach for digital filter frequency response simulation in PSpice. The PSpice analogue behaviour modelling symbol library abm.slb contains the LAPLACE part (Laplace Voltage Controlled Voltage Source), where any s-domain transfer function can be written in its numerator (NUM) and denominator (DENOM) forms. To simulate a z-domain transfer function, first, the sampling interval T should be defined in the circuit parameter list. Next, the z-domain transfer function should be written in the LAPLACE part by replacing z^n with Eq. (2). In PSpice, this replacement can be done by defining a function (Eq. (3)), and this function is the heart of the Design Idea.

```
.FUNC    z(n)    {exp(n*s*T)}          (3)
```

For example, if z(-10) is written somewhere in the numerator or denominator forms, PSpice will replace z(-10) with e^{-10sT} (s is the Laplace variable used by the LAPLACE part). Eq. (3) can be placed in an included file, or more conveniently, in the template of a new schematic part, FUNCTIONS.

The PSpice schematic for AC simulation of a digital moving-average filter is shown in Figure 1. The moving-average filters reject any signals with frequencies in the filter zeros.

For example, let the sampling frequency be f_s = 2 kHz, or T = 0.5 msec. To reject 50 Hz power-line (PL) interference, the samples from one period must be averaged. At 2 kHz sampling rate, one PL period consists of 20 msec/0.5 msec = 40 samples. The averager can be simulated directly by a transfer function (output MAV40T), or by a structure close to its real algorithmic realisation using delay blocks, gain blocks, and summing and difference junctions (output MAV40R). The simulation has notches at all harmonics of PL interference, as seen in Figure 2.

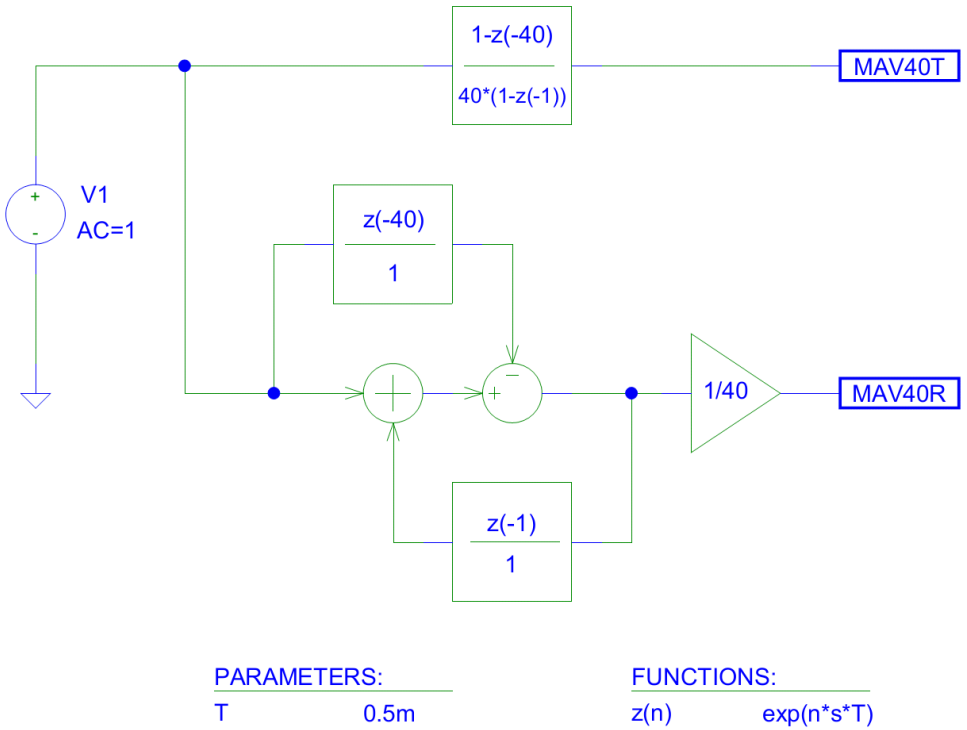


Figure 1. *PSpice schematic for AC line interference averager (comb filter)*

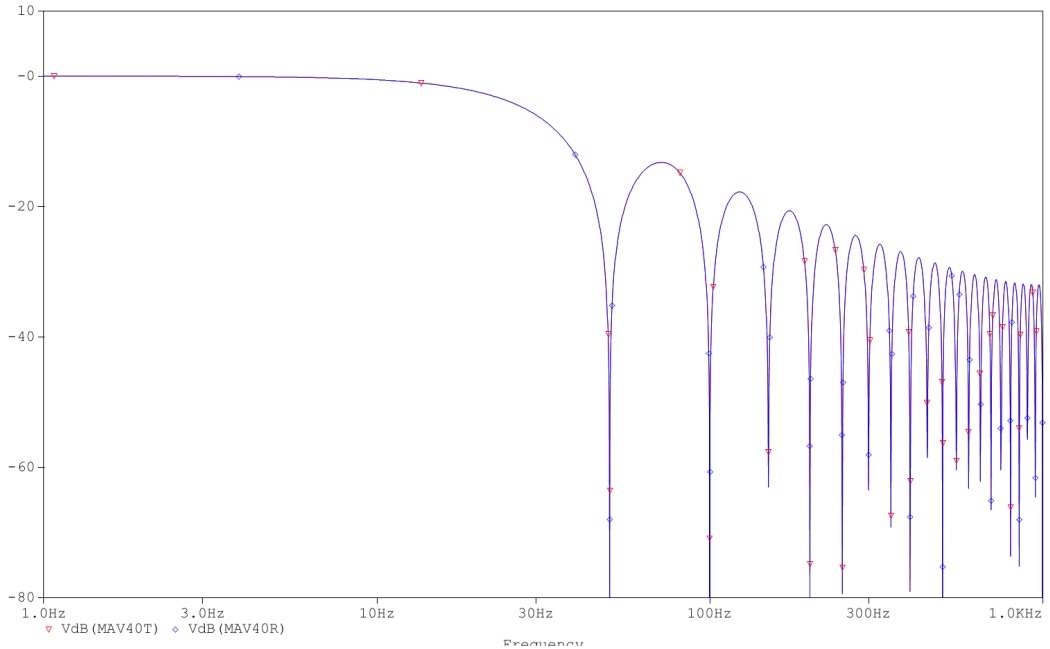


Figure 2. *Frequency response of the averager*

The presented approach is fast and easy. I have used it for 10 years, and was inspired to share my knowledge after discovering the Design Idea in Reference 1. Other examples of digital filters simulated with the presented approach can be found in Reference 2. And here are some design files.

References:

1.Lopez D., Transmission lines simulate digital filters in PSpice, EDN, 2008
2.http://www.researchgate.net/profile/Dobromir_Dobrev/publications

About the author

Dr. Dobromir Dobrev has about 20 years experience in CMOS and BJT analogue and mixed-signal IC design (opamps, comparators, bandgaps, ldos, filters, oscillators, lvdss, plls, adcs, etc.), as well as in signal processing in medical electronics (bioinstrumentation, bioamplifiers, biosignal filtering). Currently, he is with FACET (Fabless Center for Engineering and Test), and lives in Sofia, Bulgaria. You can e-mail him at dpdobrev@gmail.com

productroundup

productroundup

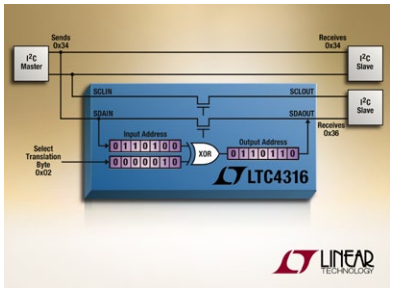
32-bit RISC IP extends use of 8051 peripherals/software

Dolphin Integration's RISC-351 Zephyr microcontroller IP (intellectual property) enables 80x51 users to benefit from 32-bit microcontroller performances while building on the i51 legacy of peripherals and software. The IP addresses applications which require high processing power with low power consumption. Dolphin Integration says it offers a smooth evolution from i51 to RISC-351, with reduction of the instruction set enabling 1 DMIPS/MHz. At the time when low power consumption is critical the yardstick of 1 DMIPS/MHz enables such an increase of performance that the frequency can be significantly reduced. RISC-351 preserves 75% of the instructions from the 80x51 family. The same peripheral access bus (SFR) with the same memory mappings enable the reuse of 8051 and 80251 peripherals at no cost.

Complete article, here

I²C bus address translators resolve address conflicts

Requiring no extra software coding or I²C multiplexers, the LTC4316/LTC4317/LTC4318 family of I²C/SMBus address translators enable multiple slaves with identical addresses, such as temperature sensors, to individually communicate with the master without conflicts. Address conflicts arise when slaves with the same hardwired address are placed on the same bus. Traditional solutions have used I²C multiplexers or switches to software-select or pin-select the slave that needs addressing. The LTC4316-18 are transparent solutions that replace I²C muxes and switches, and do not require any software programming or ENABLE control lines.



Complete article, here

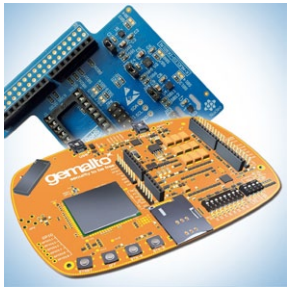
TI offers $29 package for quick IoT connection of sensors "to the cloud"

TI's claim for its SimpleLink SensorTag introduction is that users can connect sensors to the cloud in less than three minutes;10 sensors with Bluetooth Smart, 6LoWPAN or ZigBee connectivity for $29. SimpleLink SensorTag is a development kit that enables integration of sensor data with wireless cloud connectivity. Features include: multiple wireless connectivity options including Bluetooth low energy, 6LoWPAN and ZigBee; 10 integrated low-power sensors; out-of-the-box capabilities with a free iOS or Android app; connect to the cloud in less than three minutes through TI's IoT cloud ecosystem including IBM's Bluemix IoT Foundation; TI Design reference designs, including 3D print files of the SensorTag enclosures, allow reuse of the SensorTags as a starting point; a Wi-Fi demo-version of the SensorTag will be introduced soon.

Complete article, here

MEMS sensor development platform, in distribution

Distributor Anglia Components has created an evaluation platform for MEMS and environmental sensors, by linking the Cinterion Concept Board by Gemalto to an STMicroelectronics NUCLEO expansion board. Using source code supplied by Anglia, designers can request measurements such as temperature, humidity, pressure, co-ordinates and g-force from the on-board sensors using SMS communication or AT commands. The suite supports customers with the evaluation and design process by providing the tools and open source software required to facilitate further development using Java as the design environment.

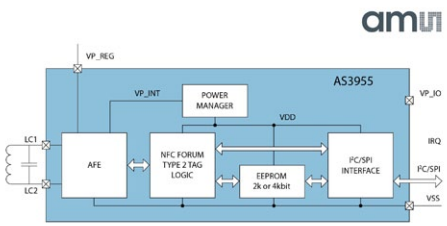


Complete article, here

productroundup

NFC to SPI/I²C NFC dynamic tag IC is NFC Forum-compliant

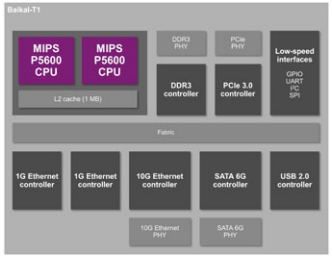
The AS3955 NFC Dynamic Tag IC adds 13.56 MHz NFC functionality to electronic devices, for example to pair them with NFC phones and transfer data. AS3955 offers standalone NFC passive tag functionality in a small footprint. Fast system integration and high speed data transfer are assisted by the availability of SPI and I²C interfaces and by optimised protocols (tunnelling mode and extended mode), allowing bidirectional communication between the device microcontroller and an external NFC compliant device or ISO14443A reader device.



Complete article, here

Comms processor from Russia based on Imagination Warrior core

Imagination Technologies has disclosed an IP design-in with its MIPS Warrior P-class CPU in the Baikal-T1 communications processor from Baikal Electronics. The low-power processor targets telecommunications, industrial automation and embedded systems. The multi-core processor from Baikal Electronics, a Russian fabless IC company, integrates Imagination's latest MIPS Warrior P-class P5600 CPU. Baikal created the Baikal-T1 with a focus on versatility, high operating frequency and low power consumption. The MIPS P5600 CPU is based on a wide issue, deeply out-of-order (OoO) implementation of the MIPS32 architecture.



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Intel "Compute Stick" with Windows 8, in distribution

Mouser Electronics has the Intel Compute Stick with Windows 8.1, which it describes as a new generation of computer from Intel. The Compute Stick enables any screen with an HDMI interface to become a fully functional personal computer. The Compute Stick comes pre-installed with the Microsoft Windows 8.1 operating system, and is a fully-functional computer in a package similar to a large USB stick. It hosts a 64-bit 1.83 GHz Intel Atom Z3735F quad-core processor with 2 Mbytes cache, integrated Intel HD graphics, and multi-channel digital audio.

Complete article, here

60V step-down controller can eliminate intermediate power buses

Intersil's ISL8117 is a 60V synchronous buck controller that can simplify power supply and distribution design; allowing for buck conversions such as 48V direct to 1V – through a very low minimum-on-time-specification – it can permit point-of-load supplies to be fed from 48V rails.
Intersil claims the device is the first 60V synchronous buck controller able to bypass the intermediate step-down conversion stage traditionally employed in industrial applications. The ISL8117 synchronous step-down PWM controller's low duty cycle (40 nsec minimum on time) enables the direct step-down conversion from 48V to a 1V point-of-load.

Complete article, here

productroundup

Infineon takes CoolMOS to generation 7; halves switching losses

Infineon Technologies' C7 series superjunction (SJ) MOSFETs is a 600 V series that claims 50% reduction in turn-off losses compared to the CoolMOS CP, offering a GaN-like level of performance in PFC, TTF and other hard-switching topologies. The company also presents it as a transition to forthcoming GaN devices. The CoolMOS C7 claims an industry first by delivering an area-specific on resistance (*A) of 1Ω per mm², extending Infineon's portfolio of products with lowest RDS(ON) per package and featuring ultra-low switching losses for high power SMPS applications such as server, telecom, solar and industrial designs.

Complete article, here

0.6 mm supercapacitors for wearable & ultra-portable devices

CAP-XX (Sydney, Australia), recently announced flat supercapacitors in the "Thinline" series of single-cell parts; the company is a maker of supercaps for burst and back-up power, and has eliminated selected materials and changed processes to reduce thickness, and cut costs to below $1. Claimed as the thinnest-available at 0.6 mm thick, and with prices starting at less than $1 in large volumes, Thinline was developed to address the size, weight and cost challenges of designing thin, sometimes disposable electronic devices for the Internet of Things (IoT).

Complete article, here

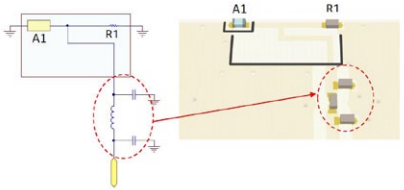
48V regulators deliver 100W from a 1-cm-square package

Vicor has added to its Picor Cool-Power ZVS regulator range with 48V buck regulators that enable direct stepdown from 48V distribution buses to point-of-load with high efficiency. Vicor says that these device increase flexibility for designers and power system architects; as well as regulated-voltage outputs, these parts can be used in a constant-current mode for applications such as LED lighting and battery management. Peak efficiency exceeding 96% is achieved at 48V to 12V stepdown. A high-density 10 x 10 x 2.5 mm LGA system in package (SiP) module handles power delivery over 100W.

Complete article, here

Ceramic antenna for 2.4 GHz consumer applications

The Weii 2.4 GHz ceramic antenna is positioned as "possibly the smallest antenna in the world" by Antenova; the miniature ceramic antenna is intended for all 2.4GHz, Bluetooth, Wi-Fi, Zigbee and ISM applications. While all of Antenova's antennas and antenna module products are small surface mounted devices, this antenna is the smallest that Antenova has created so far. It is designed specifically for the consumer, IoT and M2M markets, and measures just 1.00 x 0.5 x 0.5 mm. In the illustration above (from the component's data sheet) "A" designates the Weii device; the PCB track layout and the matching and tuning components form an intrinsic part of the device's functionality.



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productroundup

FRAM MCUs "revolutionise" context save and restore

Using the tag-line "lose power, not data", Texas Instruments has introduced ultra-low-power FRAM (ferroelectric RAM) microcontrollers that feature a facility TI calls Compute Through Power Loss (CTPL); TI aims the parts at industrial automation and metering applications, where it says they will show reduced system costs. TI says that Compute Through Power Loss technology enables context save and restore across its MSP430 FRAM microcontroller (MCU) family, including the new MSP430FR6972 MCU. The technology enables instantaneous wakeup with intelligent system-state restoration after an application unexpectedly loses power. The MSP430FR6972 MCU with TI's CTPL technology includes integrated smart analogue and digital peripherals to reduce system cost, power and size. These features include a low-power segment LCD controller, a 12-bit differential analogue-to-digital converter (ADC) with internal window comparator, and a 256-bit AES accelerator.

Complete article, here

Flexible LCD touch displays for curved surfaces

Varitronix has announced availability of a range of Ultra-Flexible LCD Displays. The displays accept a curve with a radius as tight as 12.5 cm, and currently can be manufactured in small sizes, similar to that of a credit card. The Ultra-Flexible LCD Displays use segmented monochrome TN technology and have in-cell touch capabilities. The displays have a wide operating temperature range of -10C to +60C, with a typical supply voltage of 5V. Display modes include Transmissive; Transflective; and Reflective and the inter-connection method is via heat seal FPC bonding.

Complete article, here

Wireless sensor node demonstrator hosts MAX32600 "wellness MCU"

Maxim integrated has posted details of its MAXWSNENV demo kit that provides a platform evaluating the capabilities of the environmental sensor version of Maxim's wireless sensor node (WSN). The kit provides a foundation for the Internet of Things (IoT) applications. The WSN board includes a microcontroller, Bluetooth Low Energy (BLE) transceiver, multiple environmental sensors and coin-cell holder. The WSN kit also includes a programming adapter compatible with the ARM mbed HDK specification. The microcontroller is Maxim's MAX32600, which the company terms its Wellness Measurement Microcontroller, with optimisations for biological sensing. It is an ultra-low-power ARM Cortex-M3 design with wellness sensor analogue front-end and advanced hardware security. Operating at up to 24MHz it includes 256 kB of flash memory, 32 kB of SRAM, a 2 kB instruction cache, and integrated high-performance analogue peripherals.

Complete article, here

Pocket-sized fanless PC hosts 4-core AMD CPU

TinyGreenPC has a fully upgradeable and expandable fanless PC offering four times the performance and memory capacity of the previous fanless FitPC2 in a unit 30% smaller. This fitlet is also 4 times faster than the Intel NUC currently on the market. Based on an AMD Quad Core processor, the fitlet offers a high level of expandability for a pocket-size fanless PC. The central feature of fitlet is its FACET interface (Function and Connectivity T-card). This interface provides 3PCIe lanes, USB and LPC bus on a standard mini-PCIe connector, giving freedom to OEMs to tailor the PC to their needs.

Complete article, here

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